DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

Lecture #3

Introduction

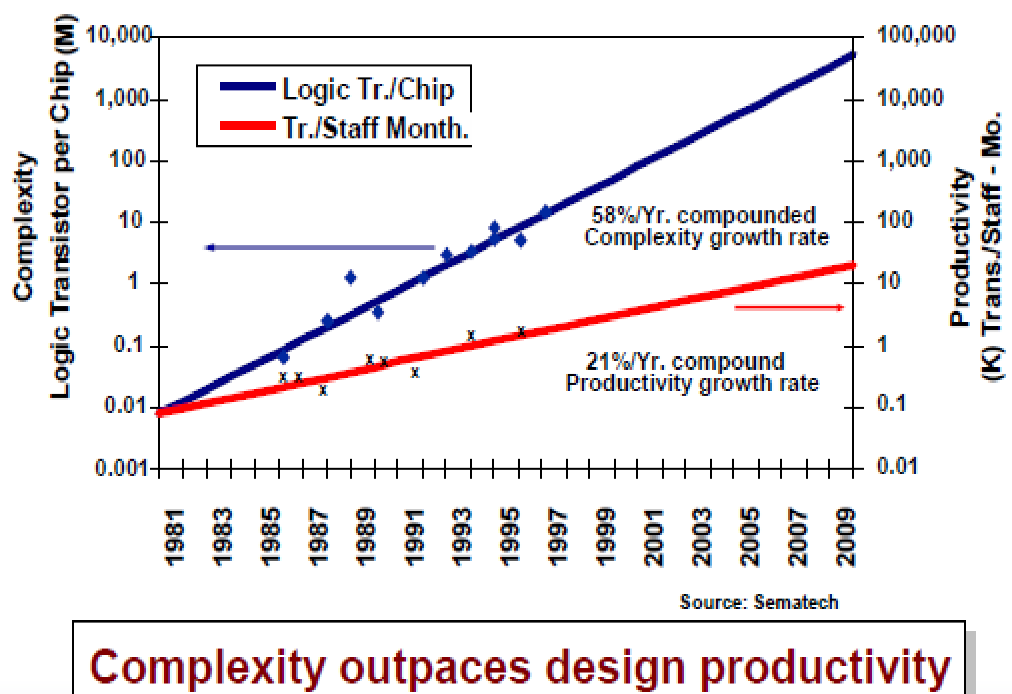
IC Manufacturing and Design Metrics CMOS

Digital Integrated Circuits

	Course topics and Schedule
	Subject
1	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design The CMOS inverter
5	Combinational logic structures
6	Sequential logic gates; Latches and Flip-Flops
7	Layout of an Inverter and basic gates
8	Parasitic Capacitance Estimation
9	Device modeling parameterization from I-V curves.
	Short Test
10	Arithmetic building blocks
11	Interconnect: R, L and C - Wire modeling
12	Timing
	Power dissipation;
13	SPICE Simulation Techniques (Project)
14	Memories and array structures
	Midterm
15	Clock Distribution
16	Supply and Threshold Voltage Scaling
17	Reliability and IC qualification process
18	Advanced Voltage Scaling Techniques
19	Power Reduction Through Switching Activity Reduction
20	CAD tools and algorithms
21	Final & Project discussion

Productivity Trends

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more
- functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- How to design chips with more and more functions?
- Design engineering population does not double every two years…
- Need to understand different levels of abstraction



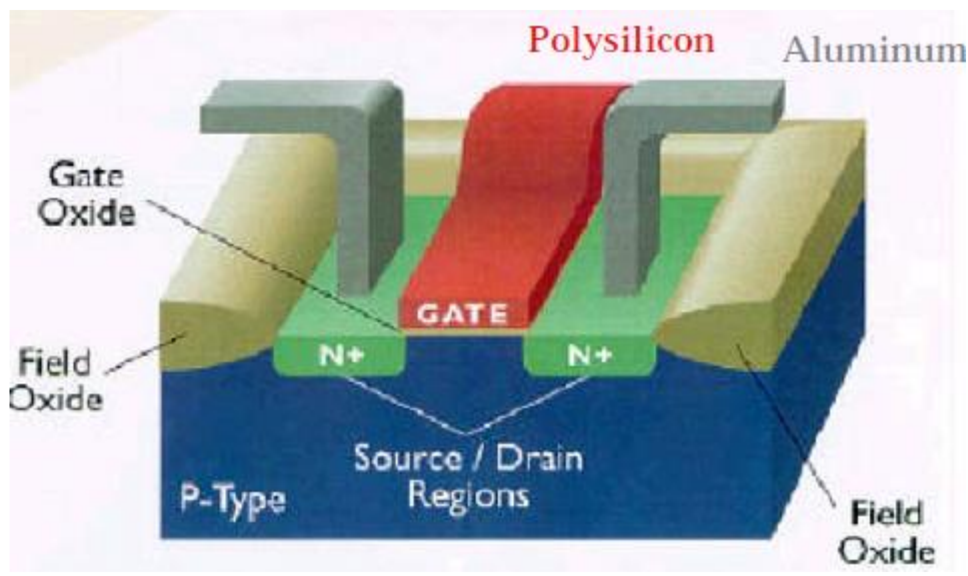
IC Manufacturing Process

Largest IC Foundries

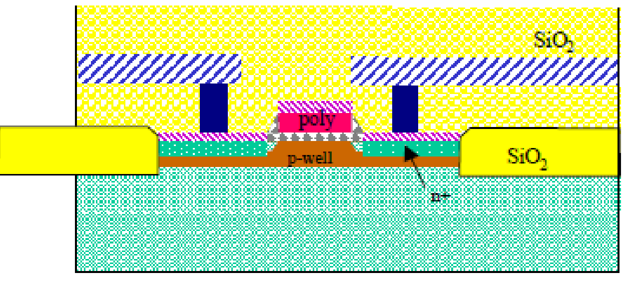
TSMC	Taiwan Semiconductor Manufacturing Company
GF	Global Foundries
UMC	United Microelectronics Corporation
Samsung	Samsung
SMIC	Semiconductor Manufacturing International Corporation
TowerJazz	Tower Semiconductor
ELMOS	Elmos Semiconductor AG
XFAB	Mixed-Signal Foundry Expert

The MOS Transistor

- ***3D Perspective***



Cross-Sectional View



Transistor Layout

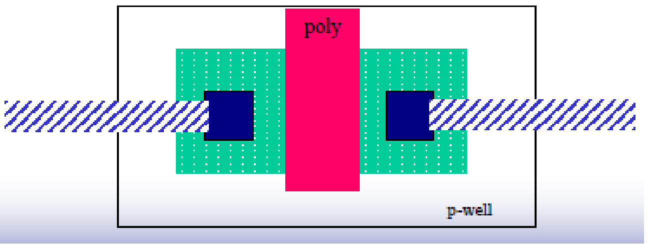


Photo-Lithographic Process

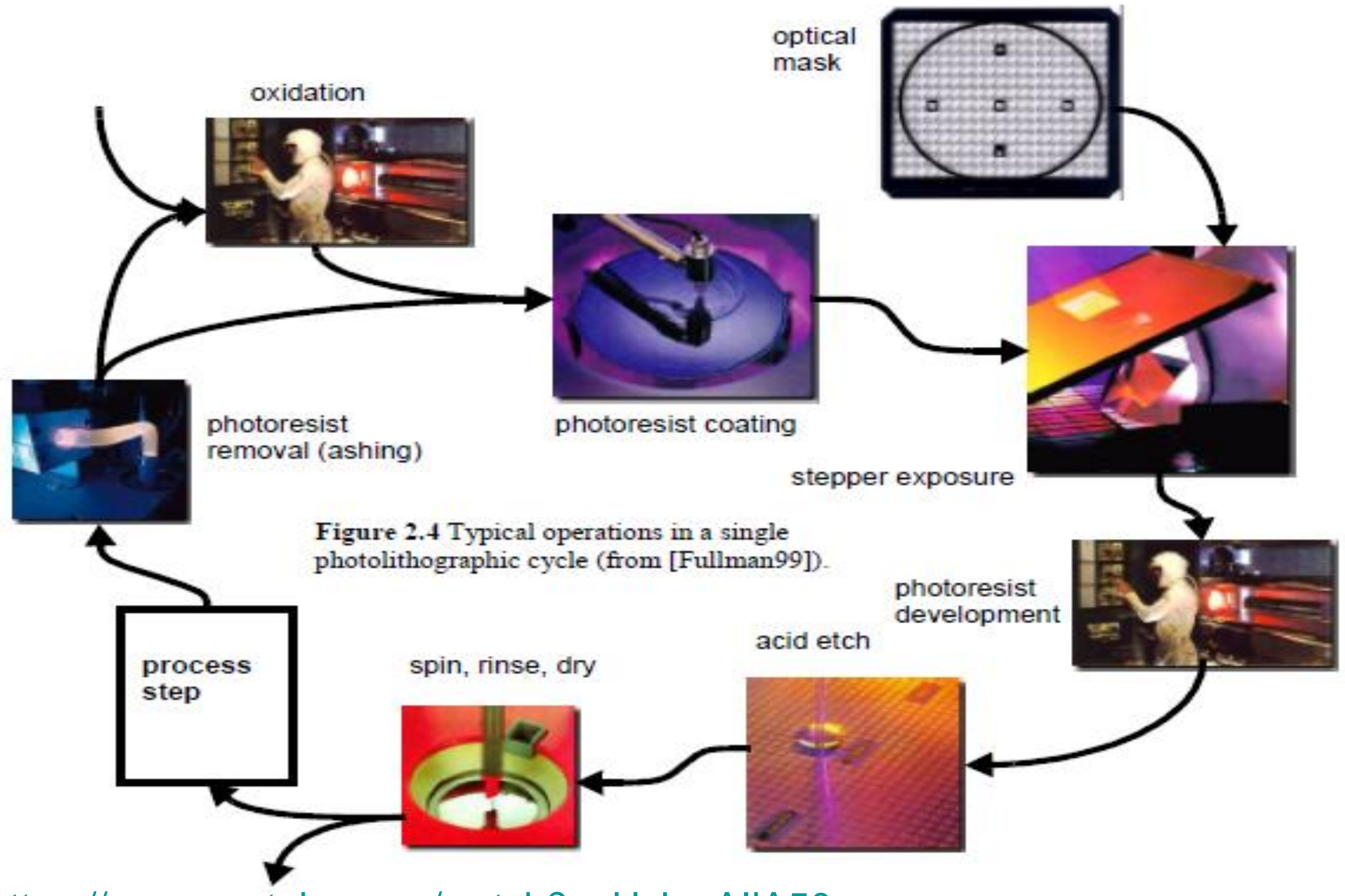
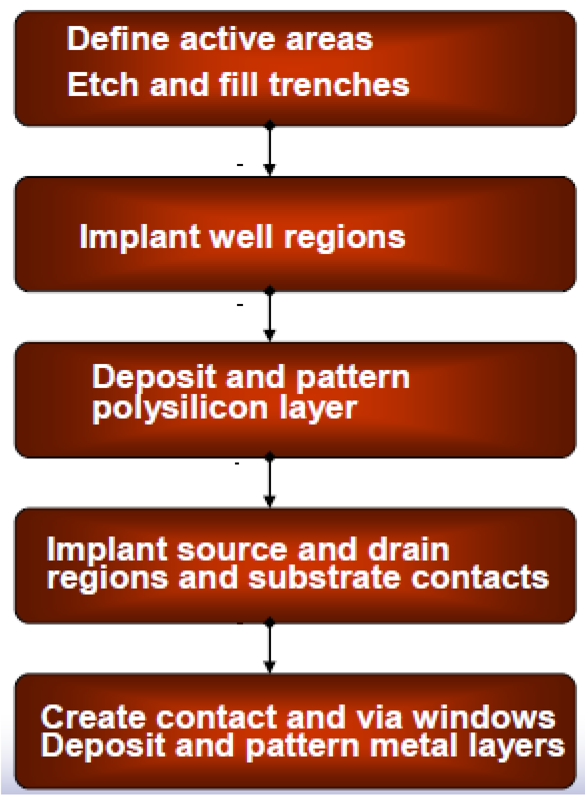


Figure 2.4 Typical operations in a single photolithographic cycle (from [Fullman99]).

https://www.youtube.com/watch?v=UvluuAIiA50

https://www.youtube.com/watch?v=_bhEDQzNQ-c

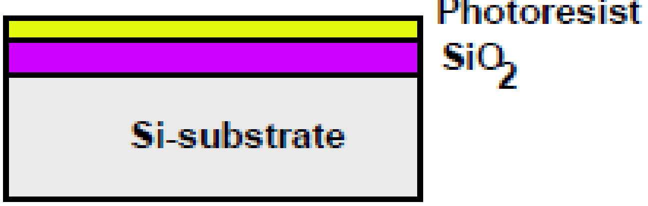
CMOS Process



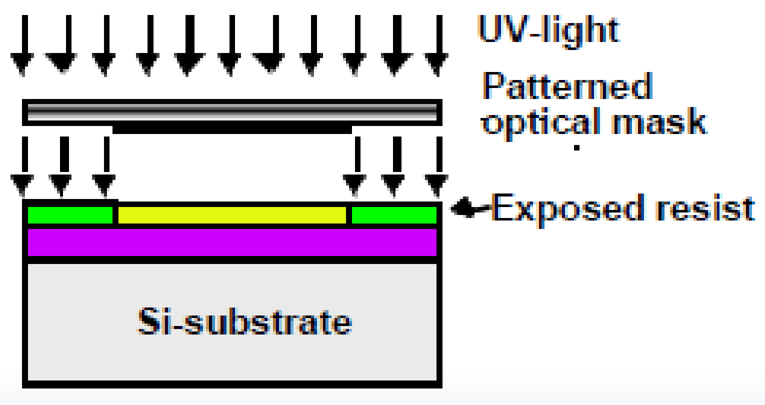
Patterning of SiO2

Si-substrate

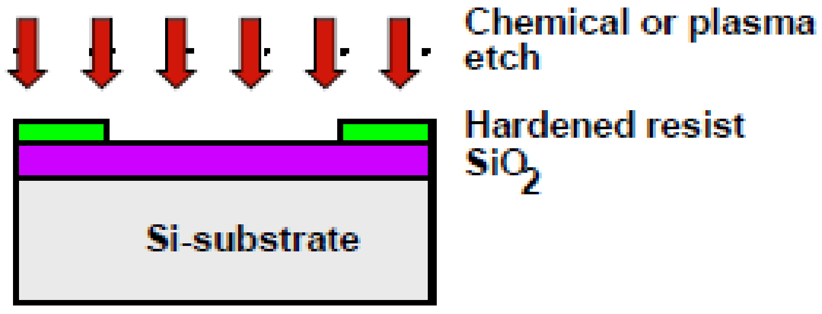
(a) Silicon base material



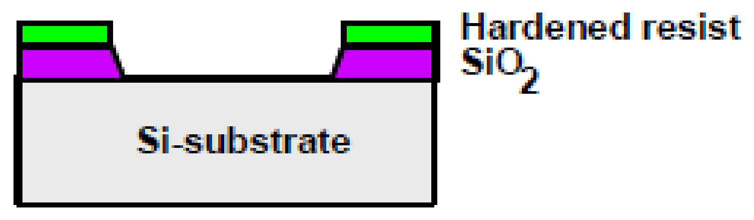
(b) After oxidation and deposition of negative photoresist



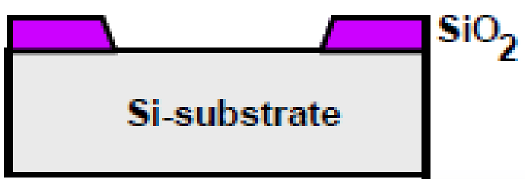
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2



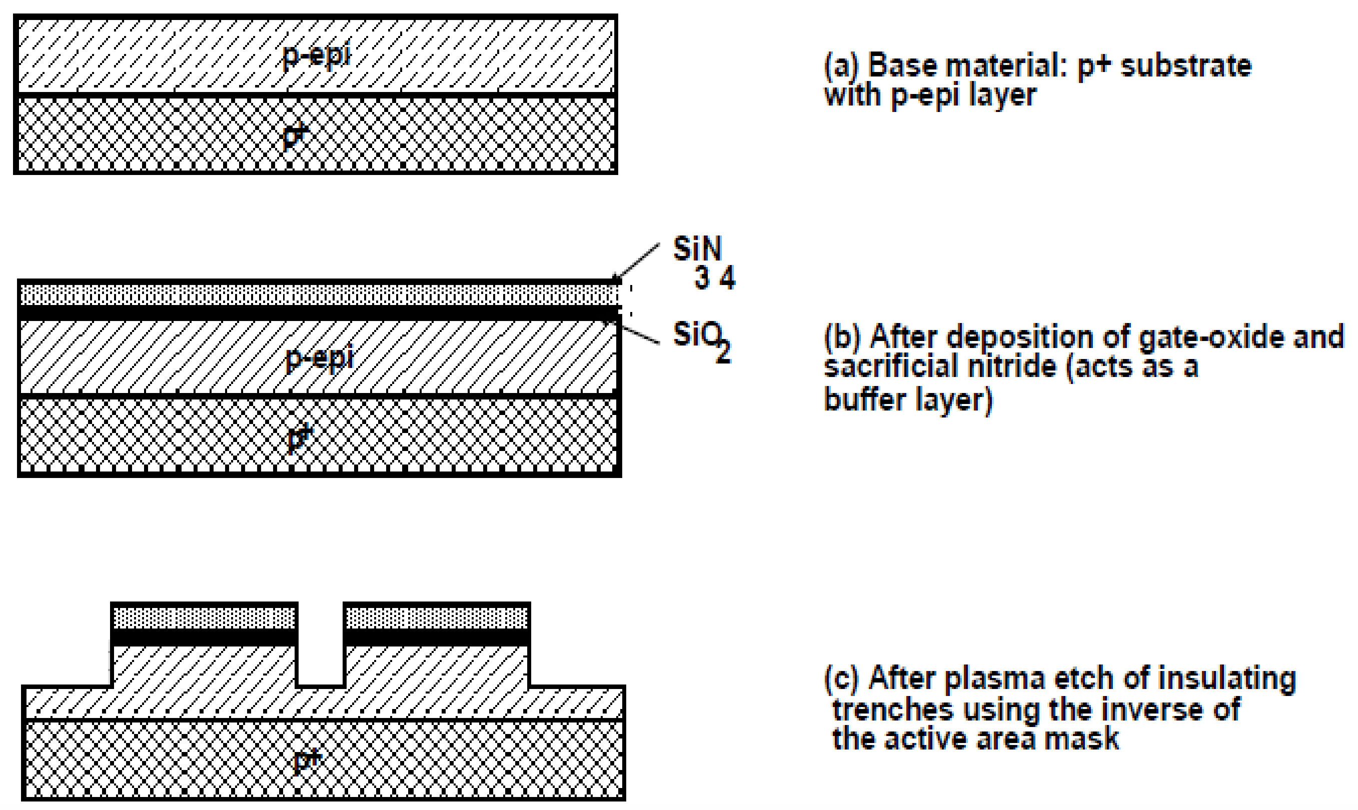
(e) After etching



(f) Final result after removal of resist

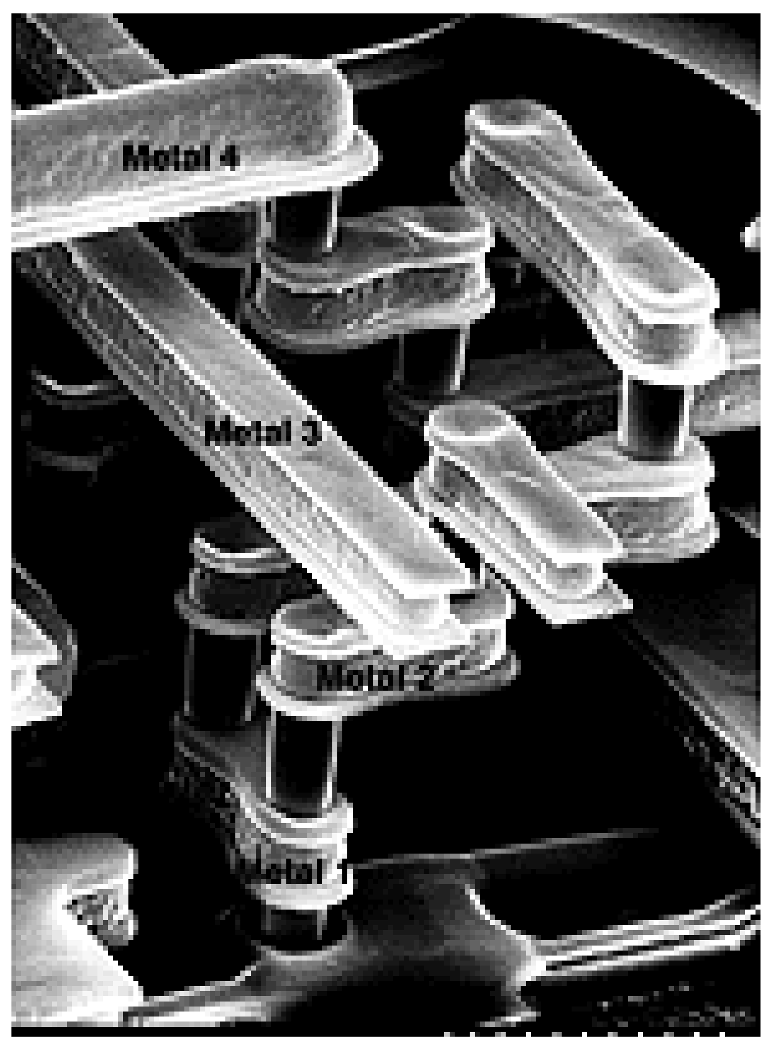
CMOS Process Walk-Through

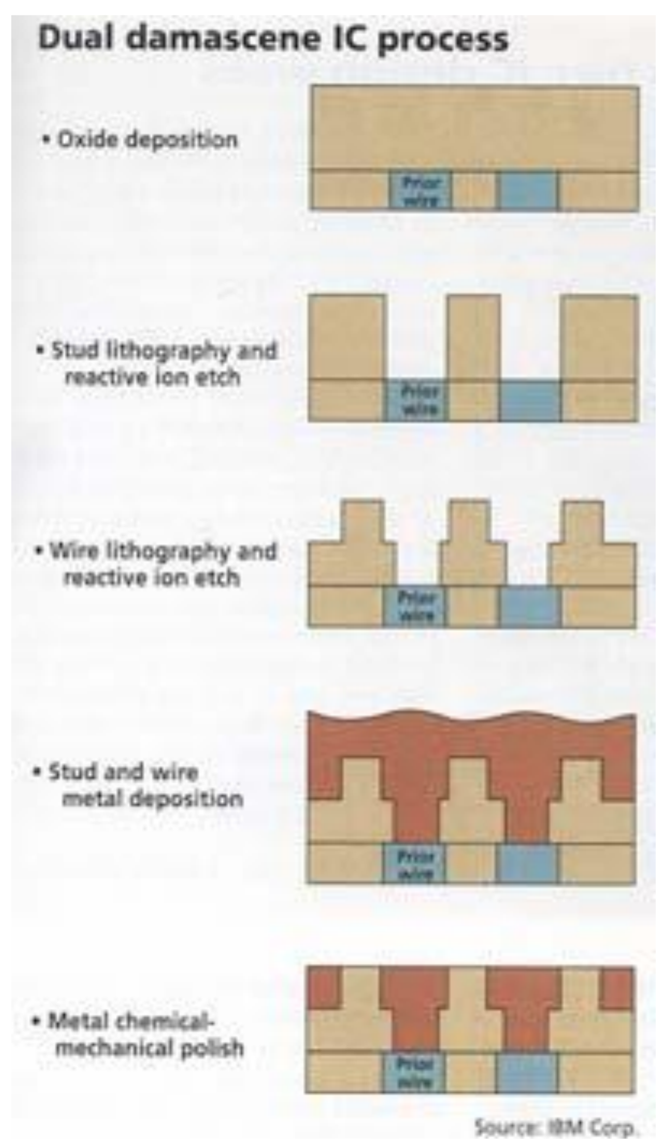
- Please read the rest from the book (process engineer)



Advanced Metallization

- Real Image from silicon



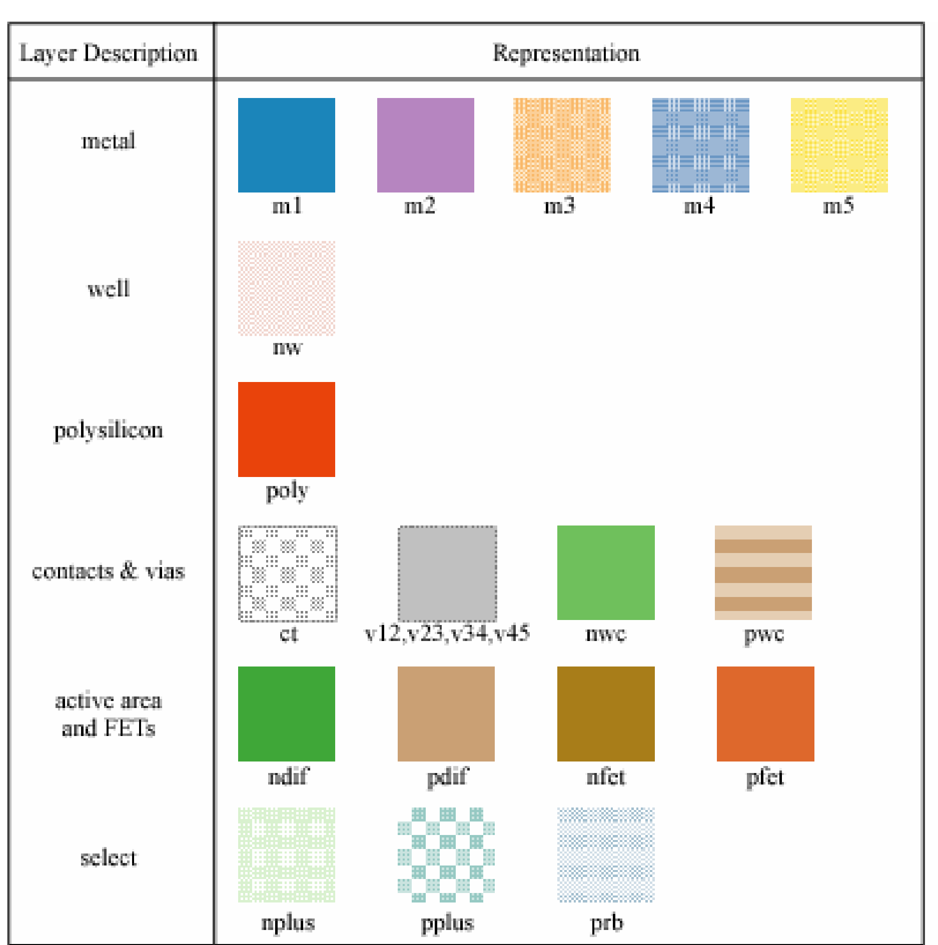


Design Rules

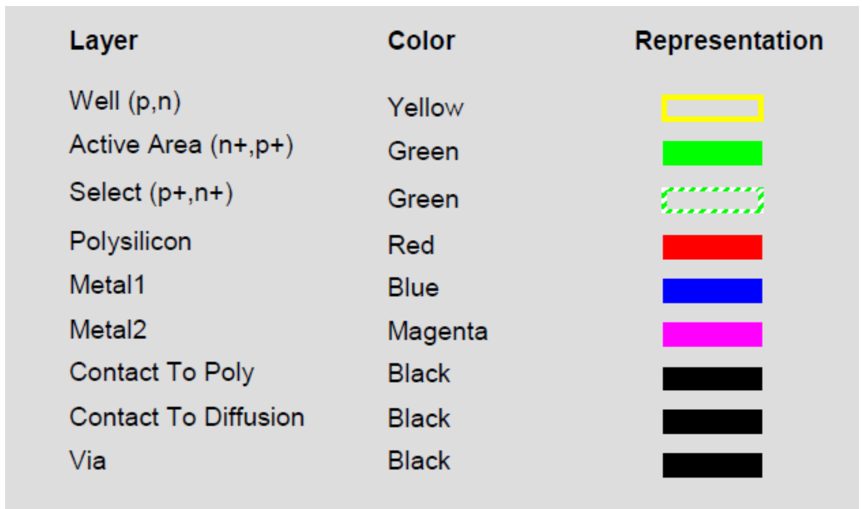
- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
- scalable design rules: lambda parameter
- absolue dimensions (micron rules)

CMOS Process Layers

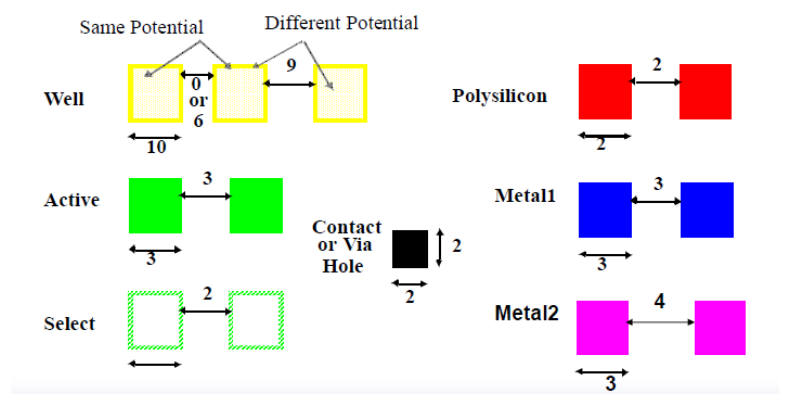
- *Layers in 0.25 µm CMOS process*



Layer Description	Representation
metal	m1, m2, m3, m4, m5
well	nw
polysilicon	poly
contacts & vias	ct, v12,v23,v34,v45, nwc, pwc
active area and FETs	ndif, pdif, nfet, pfet
select	nplus, pplus, prb

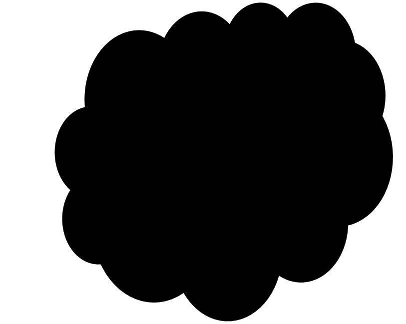


Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	



We will talk more a bout this in layout section in the coming lectures

Video



- Sand to silicon
- https://www.youtube.com/watch?v=qm67wbB5GmI

https://www.youtube.com/watch?v=gcIWcX3G6-U

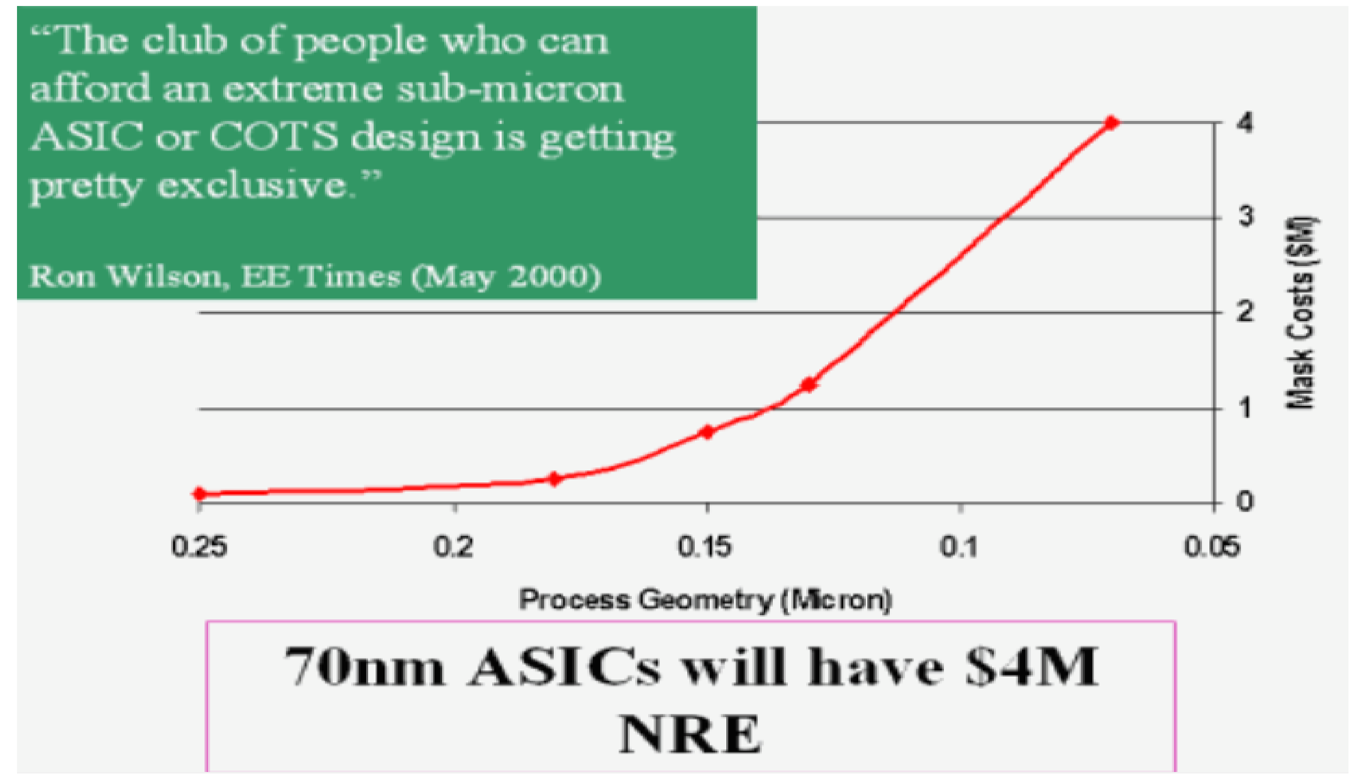
https://www.youtube.com/watch?v=NKYgZH7SBjk

Design Metrics

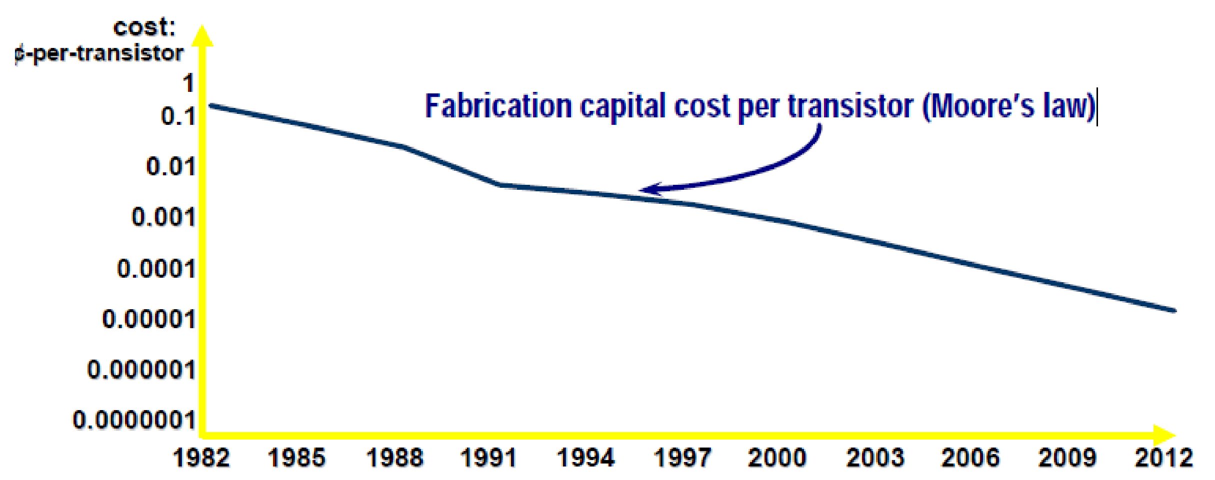
- How to evaluate performance of a digital
- circuit (gate, block, …)?
  - Area/Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

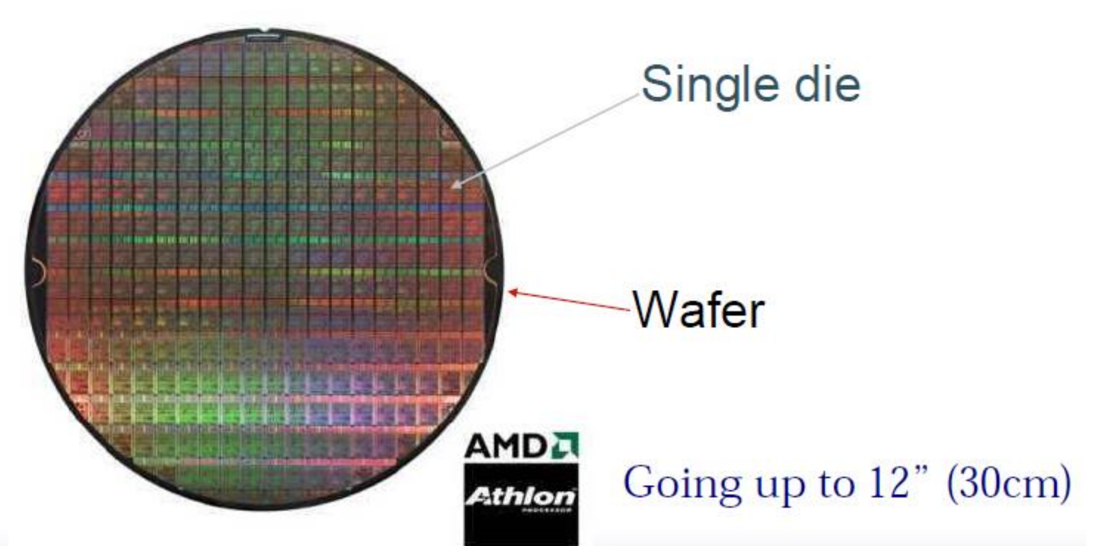
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area current costs



Die Cost & Cost per Transistor



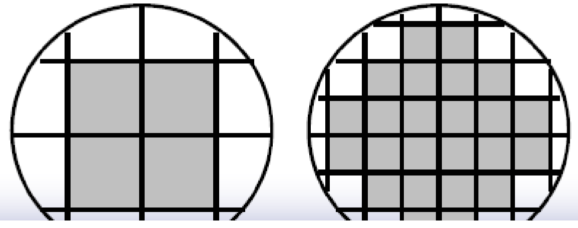


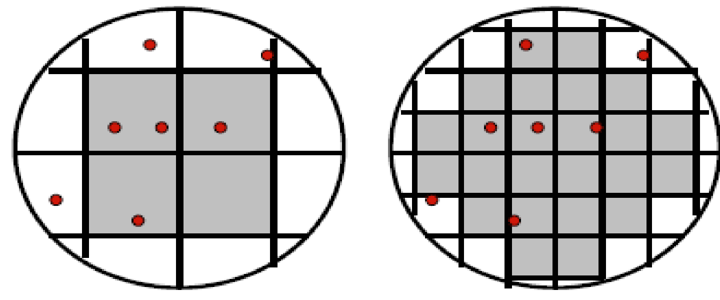
Yield & Defects

$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$





$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

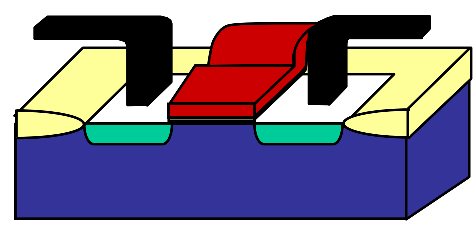
$$\text{die cost} = f(\text{die area})^4$$

Some Examples (1994)

Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Evaluation of Technological Processes

Technological processes are defined by the minimum length (L) of CMOS transistor channel



90nm technology – Lmin=90nm

45nm technology – Lmin=45nm

22nm technology – Lmin=22nm

Examples of technological processes:

- TSMC 90nm G Logic 1.0V/3.3V
- SMIC 90nm LL Logic 1.2V/3.3V
- SMIC 130nm LV Logic 1.0V/3.3V
- Samsung 90nm LP Logic 1.2V/3.3V
- UMC 90nm LL Logic 1.2V/2.5

G – generic

LL – low leakage

LV – low voltage

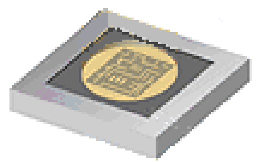
LP – low power

IC Fabrication at a Glance

- Growing of a giant crystal of silicon

- Slicing it up into round wafers and polish them

- Coating of a wafer with a photographic chemical that hardens when exposed to light
- Taking a picture of a pattern to embed in the silicon



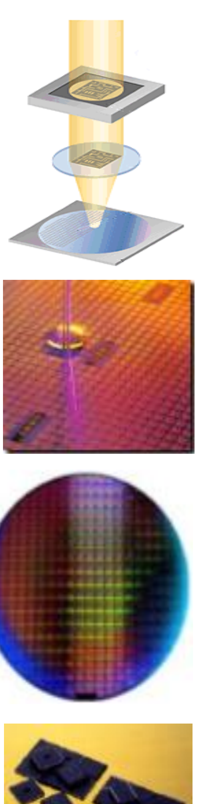
IC Fabrication at a Glance (2)

- Shrinking of the picture and shining a light through it

- Dipping of the wafer in acid to etch away the soft parts
- Repetition of steps 3 - 6 many times, producing layers of patterns etched into the wafer

- Cut up of the wafer into many rectangle chips

- Gluing of the chip into a plastic package



IC Fabrication at a Glance (3)

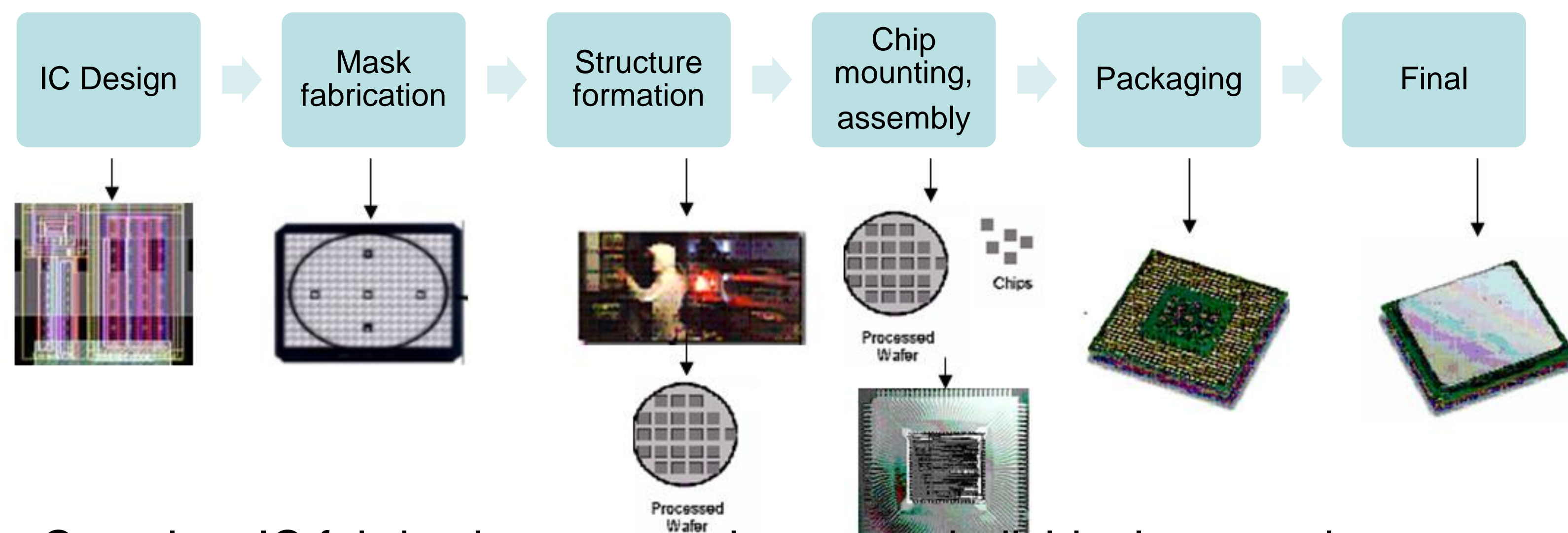
- Connection of chip parts to the pins of the package with tiny gold wires

- Putting of the chip on a tester machine and test running

- Assembly of different kinds of chips onto a board

- Installation of the board into a phone, computer...

General Technology Flow Diagram



- Complete IC fabrication process has many individual processing steps (>100) and can take several weeks to carry out.
- Each process step is accurately controlled in order to give acceptable overall result (high process yield).

Fabrication: Key Requirements

- General
  - High reliability
  - Cost effectiveness
  - Safeness for personal and environment
  - High reproducibility
- Private
  - High purity materials and reagents are needed
  - Manufacturing process carried out in clean rooms and local volumes, which is extremely important
  - Contamination control in clean rooms

Examples of Devices Used During IC Fabrication

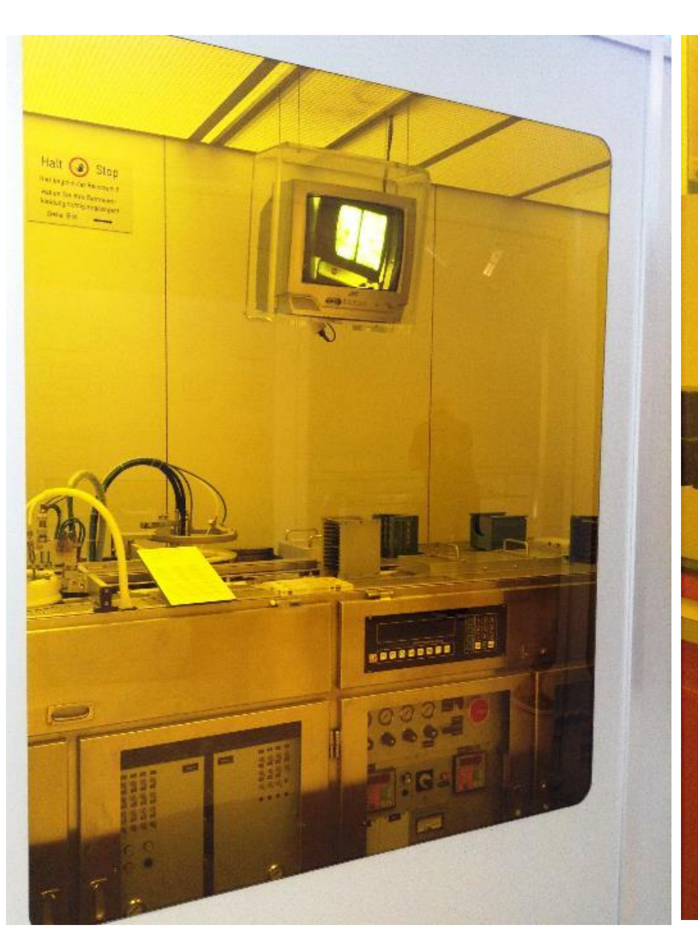
Photolithography stepper

Gas cabinet

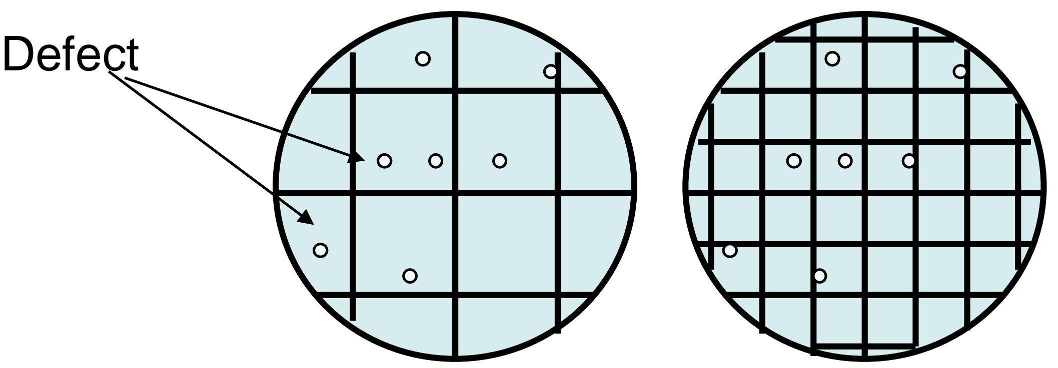
Wire bonder system

Wafer probe

Examples of Devices Used During IC Fabrication (2)



Defects and Yield



$$\text{Yield} = \frac{\text{Number of working dies}}{\text{Number of all manufactured dies}} .100\%$$

Clean Rooms

- IC Fabrication requires special conditions
- Rooms with fabrication equipment should be clean of particles

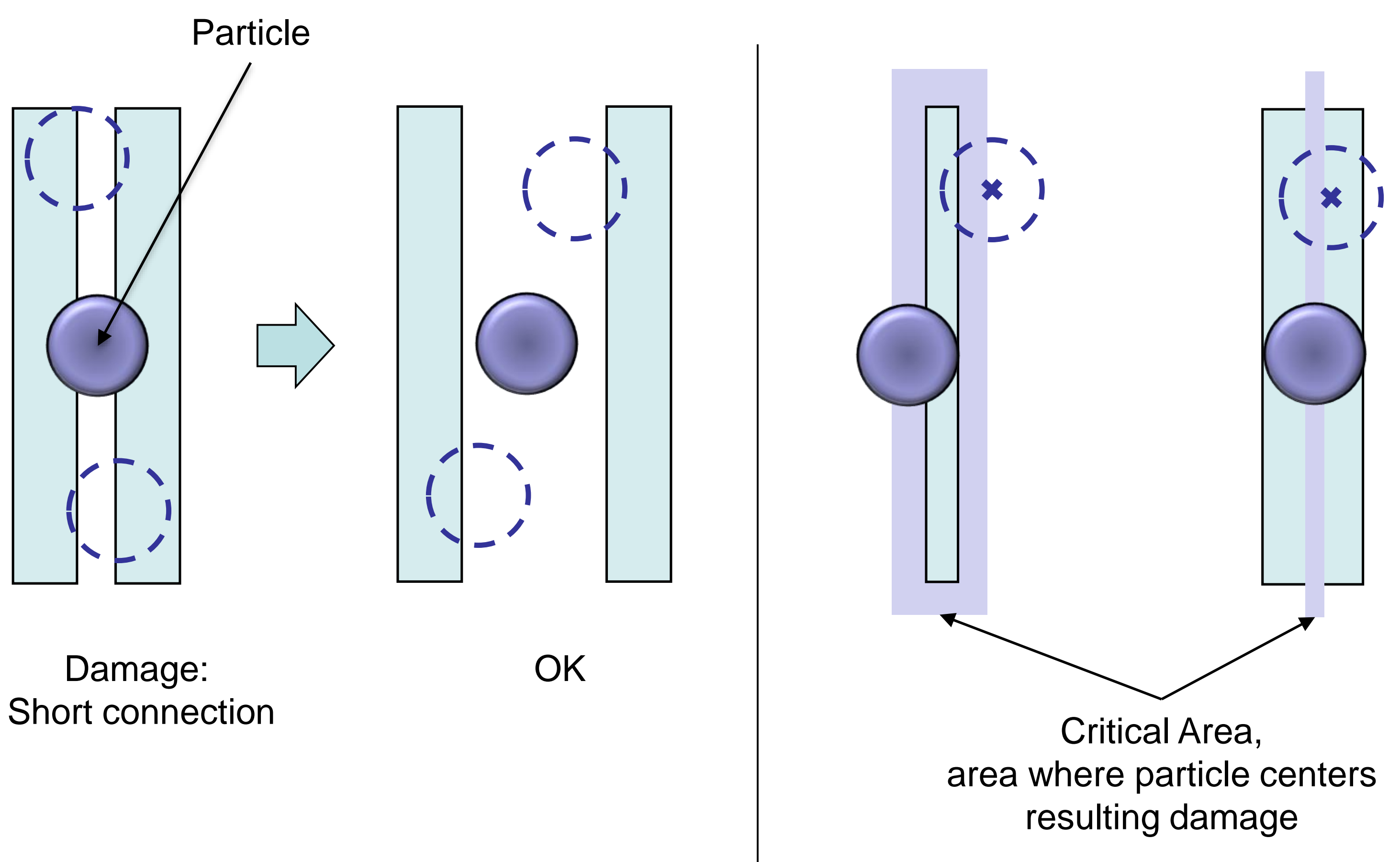
Class	maximum particles/m³		
	≥0.1 µm	≥0.3 µm	≥5 µm
ISO 1	10	1.02	0.0029
ISO 2	100	10.2	0.029

TSMC's 12-inch Gigafab™

- Cost: $9.3b
- Total area of site: 184,000 m^2
- Building area: 430,000 m^2
- Clean room area: 104,000 m^2

Source: Engadget

Design Solution for Yield



Lithography

Silicon Technology ≡ Lithography

- Lithography is a basic method of IC fabrication process.
- Process is used to transfer patterns from masks to each layer of the IC on the surface of a wafer by employing a photosensitive, chemically resistant layer (photoresist).
- Masks are created using the layout information provided by the designer.
- The lithographic process is repeated for each physical layer, but the process sequence is always the same:

- Photoresist application
- Exposure (contact or projection)
- Development
- Etching

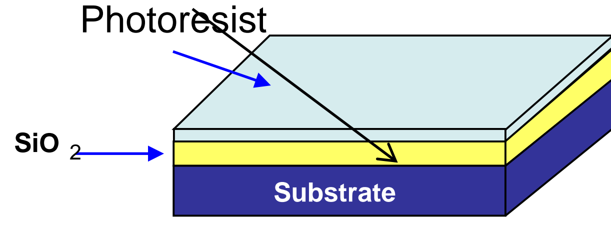
Photolithographic Process

https://www.youtube.com/watch?v=AMgQ1-HdElM

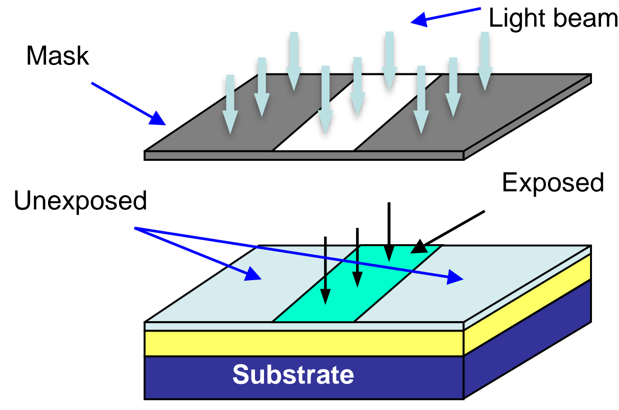
https://www.youtube.com/watch?v=UvluuAIiA50

Steps of Photolithography

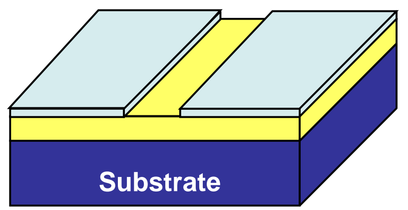
1 **Photoresist coating**



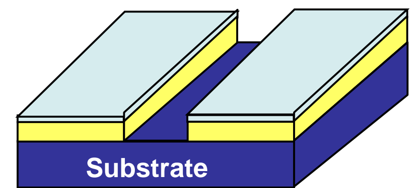
2 **Exposure**



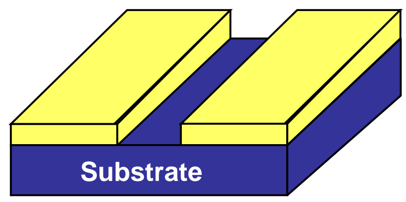
3 **Development**



4 **Etching**

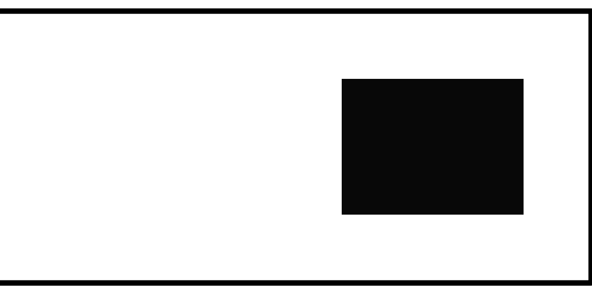


5 **Photoresist removal**



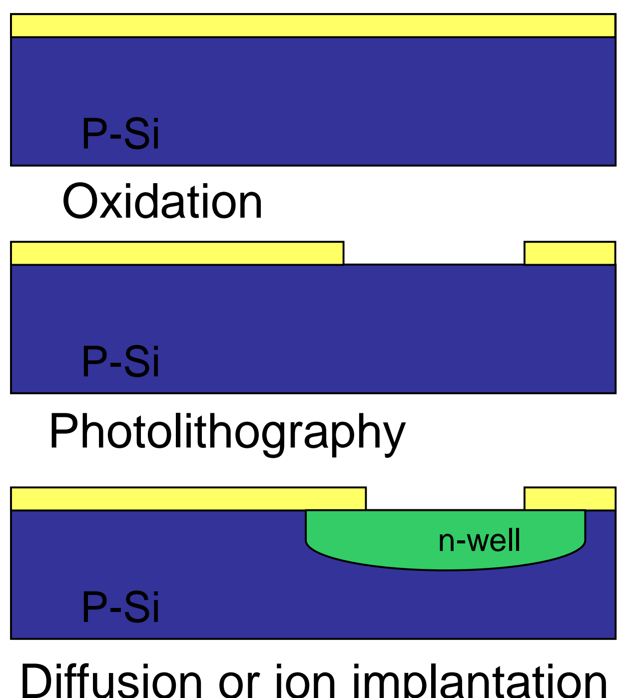
Mask Types

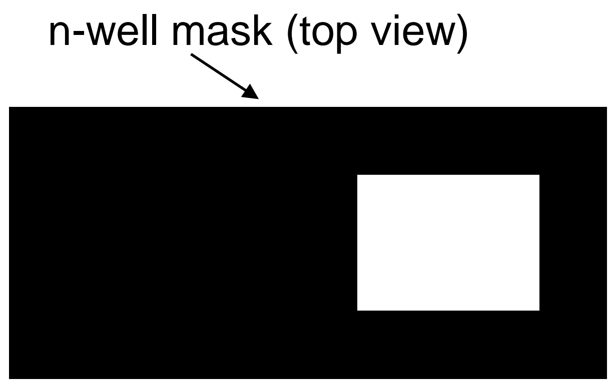
- Masks can be negative or positive depending of the type of photoresist material



Mask Example

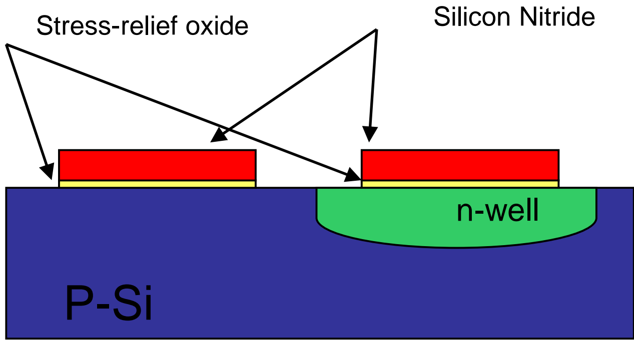
- N-well Process mask

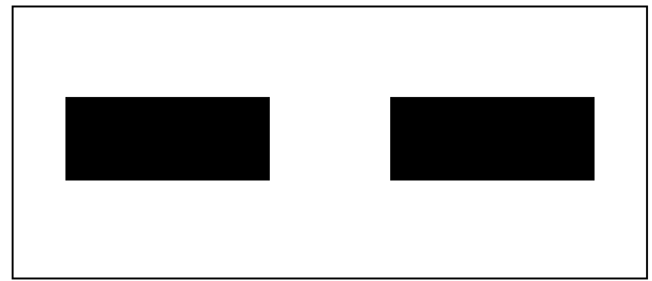




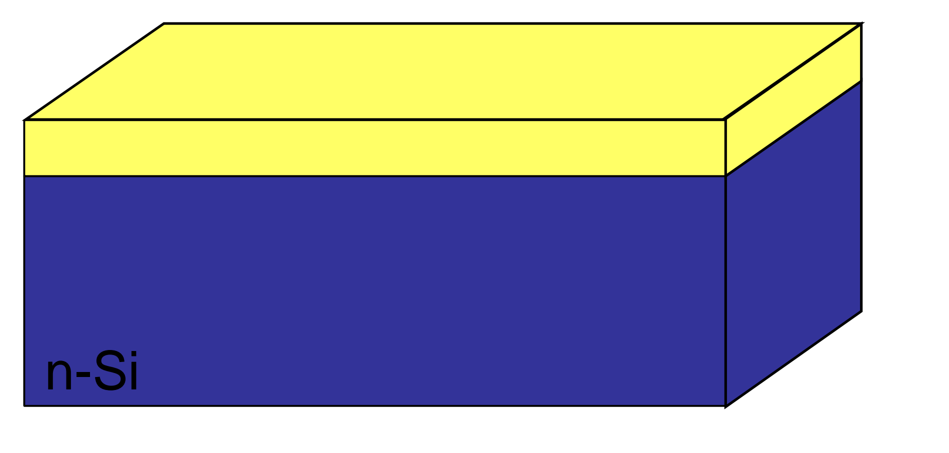
Mask Example (2)

- Gate mask

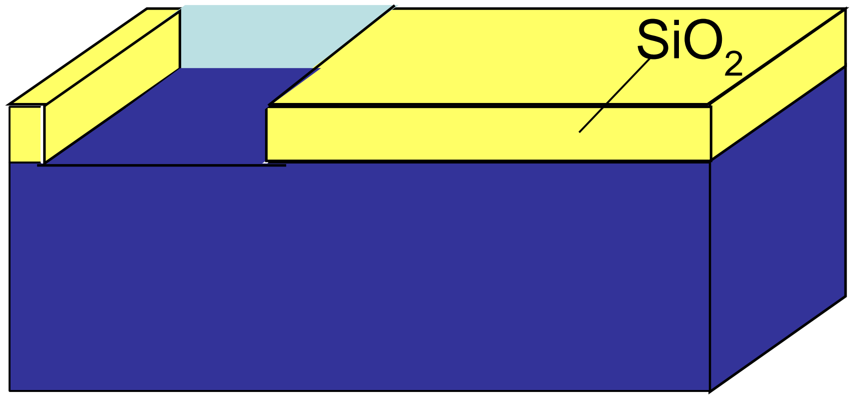




Fabrication Process

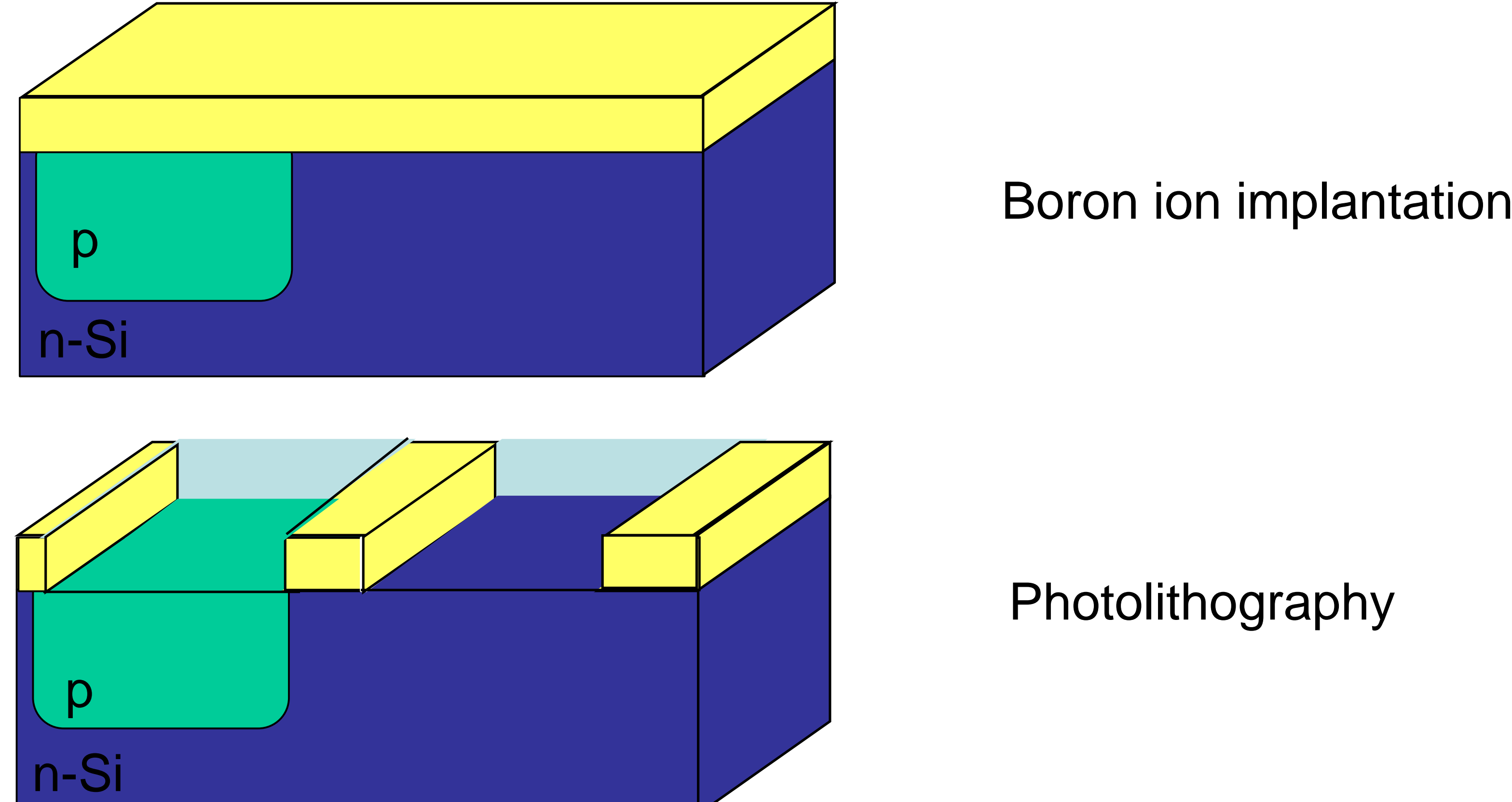


Thermal oxidation

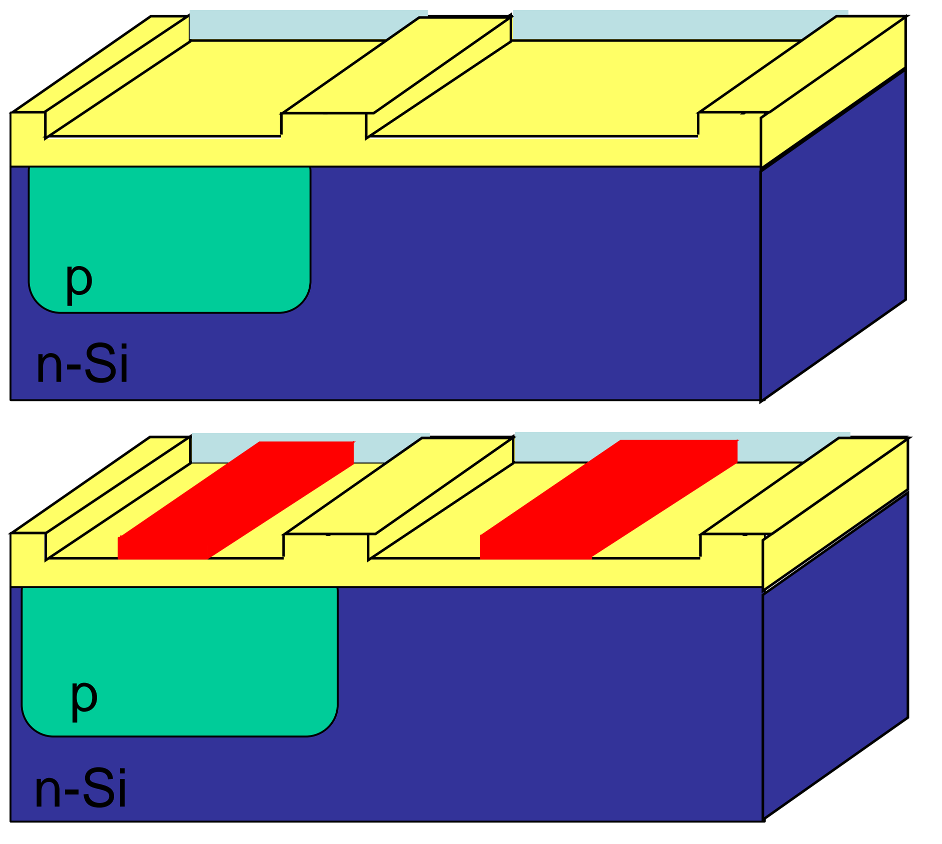


Photolithography

Fabrication Process (2)



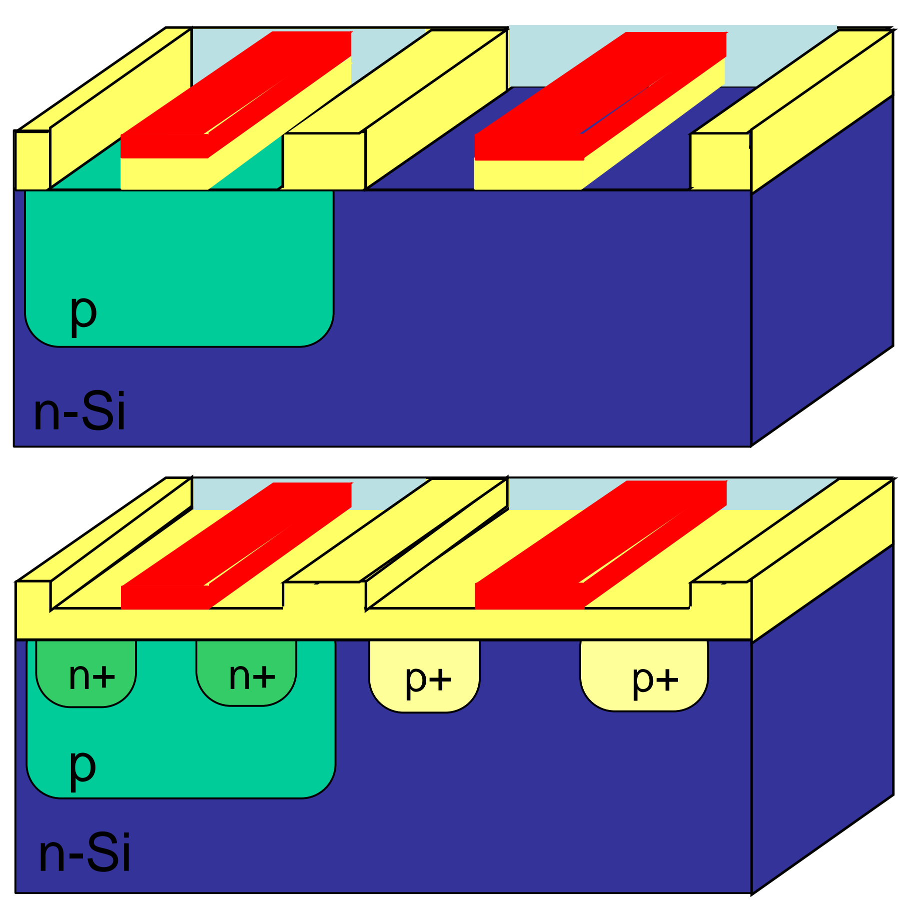
Fabrication Process (3)



Gate oxide formation (SiO_2)

Polysilicon deposition, photolithography (gates and wires)

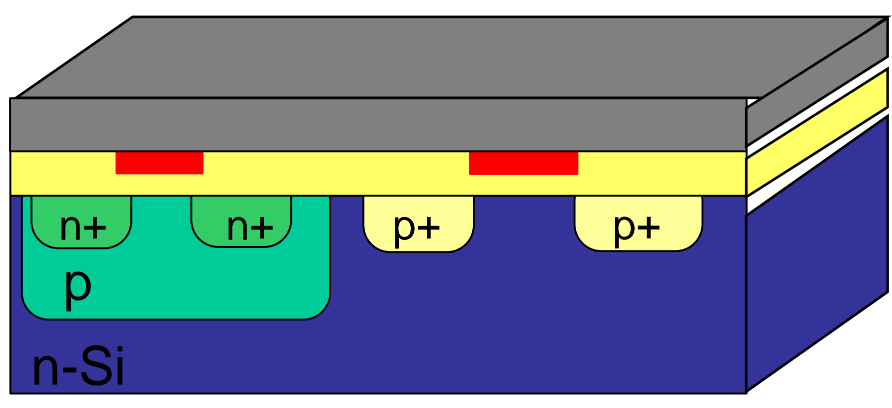
Fabrication Process (4)



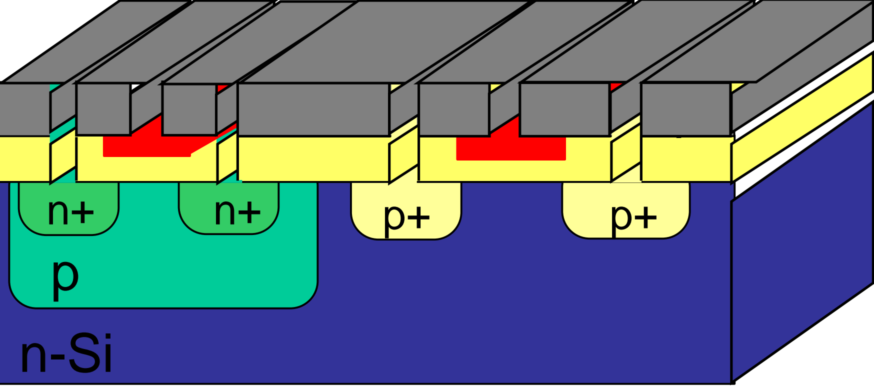
Photolithography

Oxidation and sequentially accepter and donor ion implantation

Fabrication Process (5)

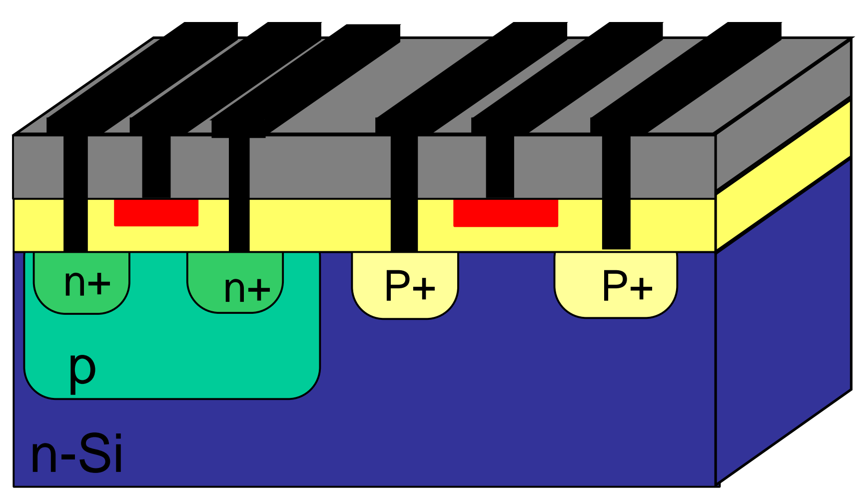


Glass deposition (interlayer isolation)



Contact windows formation

Fabrication Process (6)



Metal layer deposition (Al, Cu) and photolithography

Mask Data Generation

- Mask data, used in CMOS process, can be generated by a Layout Editor tool (for example, Custom Compiler LE).
- Layout design rules: There are constraints on the shape, size and spacing of the layer. The objective is to obtain a circuit with the best possible compromise between performance and yield.
- Example processes. Each has its own design rules.
  - TSMC 90nm G Logic 1.0V/3.3V
  - SMIC 90nm LL Logic 1.2V/3.3V
  - SMIC 130nm LV Logic 1.0V/3.3V
  - Samsung 90nm LP Logic 1.2V/3.3V
  - UMC 90nm LL Logic 1.2V/2.5

G – generic
LL – low leakage
LV – low voltage
LP – low power

Abstract Layers

- CMOS process is complex
- Hard to draw all masks during the layout design
- Masks are represented by a few number of layout levels (abstract layers)
- Abstract layer are represented by:
  - Color scheme
  - Stipple patterns
  - Line styles
- Layer assignments:
  - Layers are converted to mask data

Layers

VDD

metal1

polysilicon

m1diffcont

metal1(out)

m1polycont (in)

m1diffcont

PDIFF

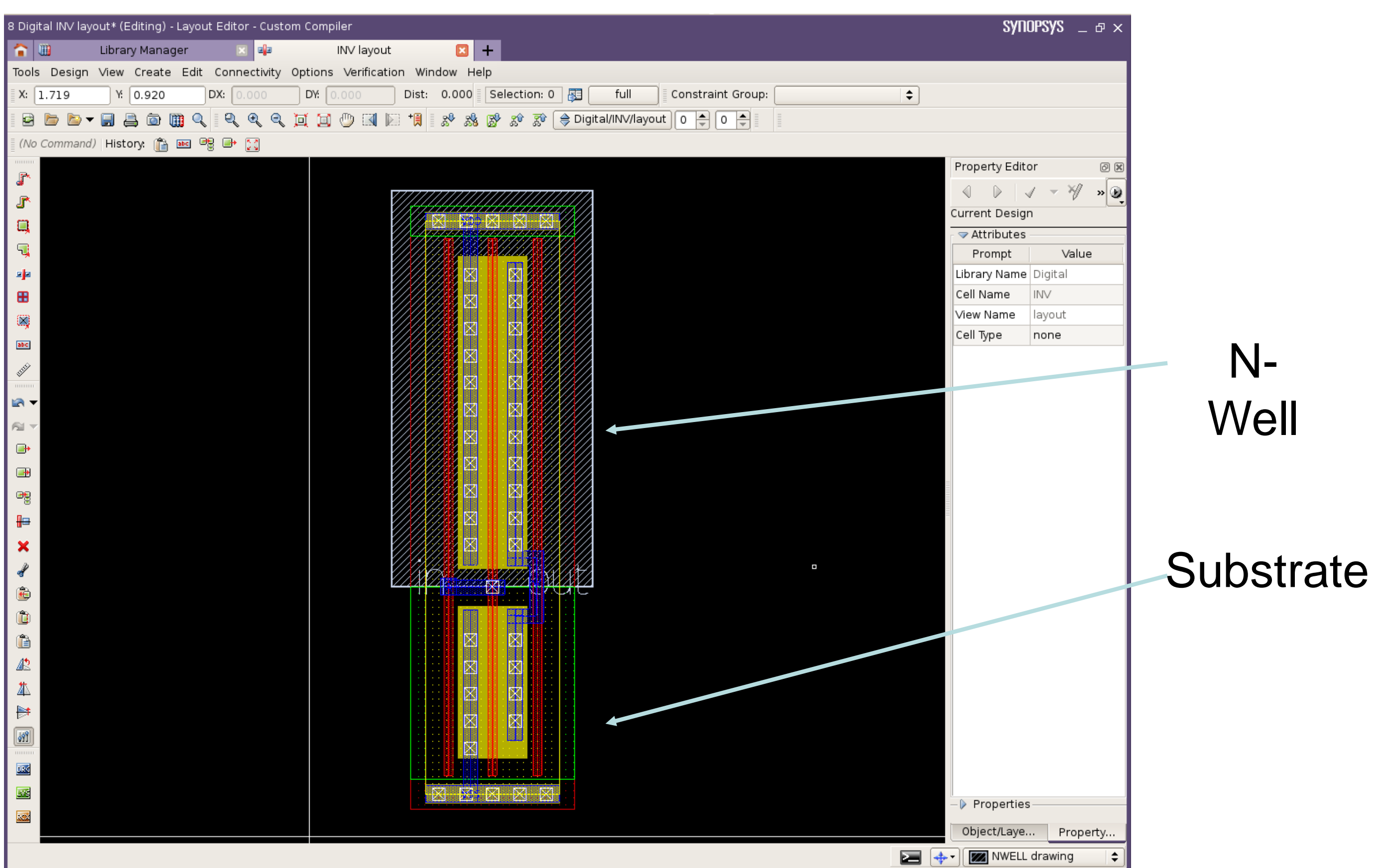
PMOS

NMOS

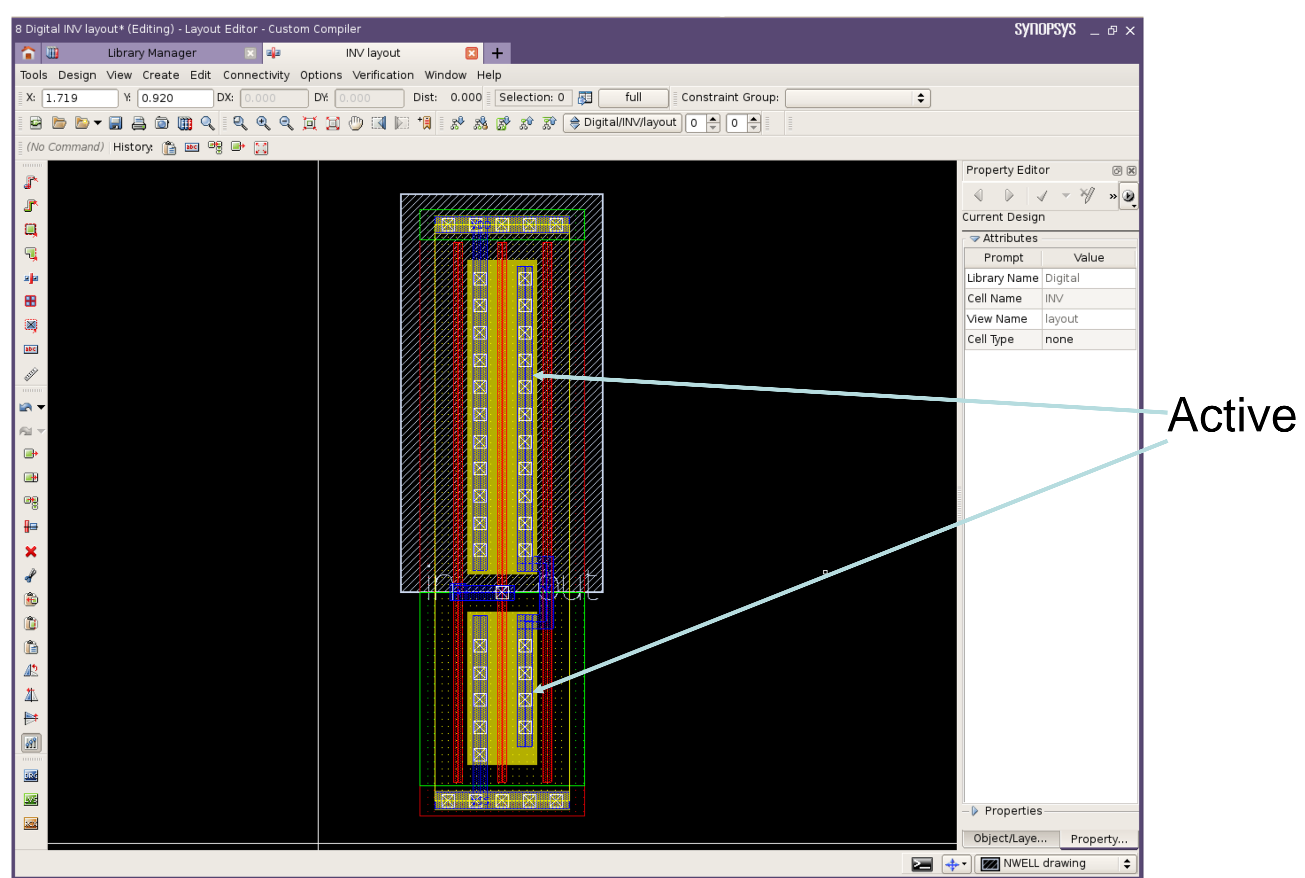
NDIFF

VSS

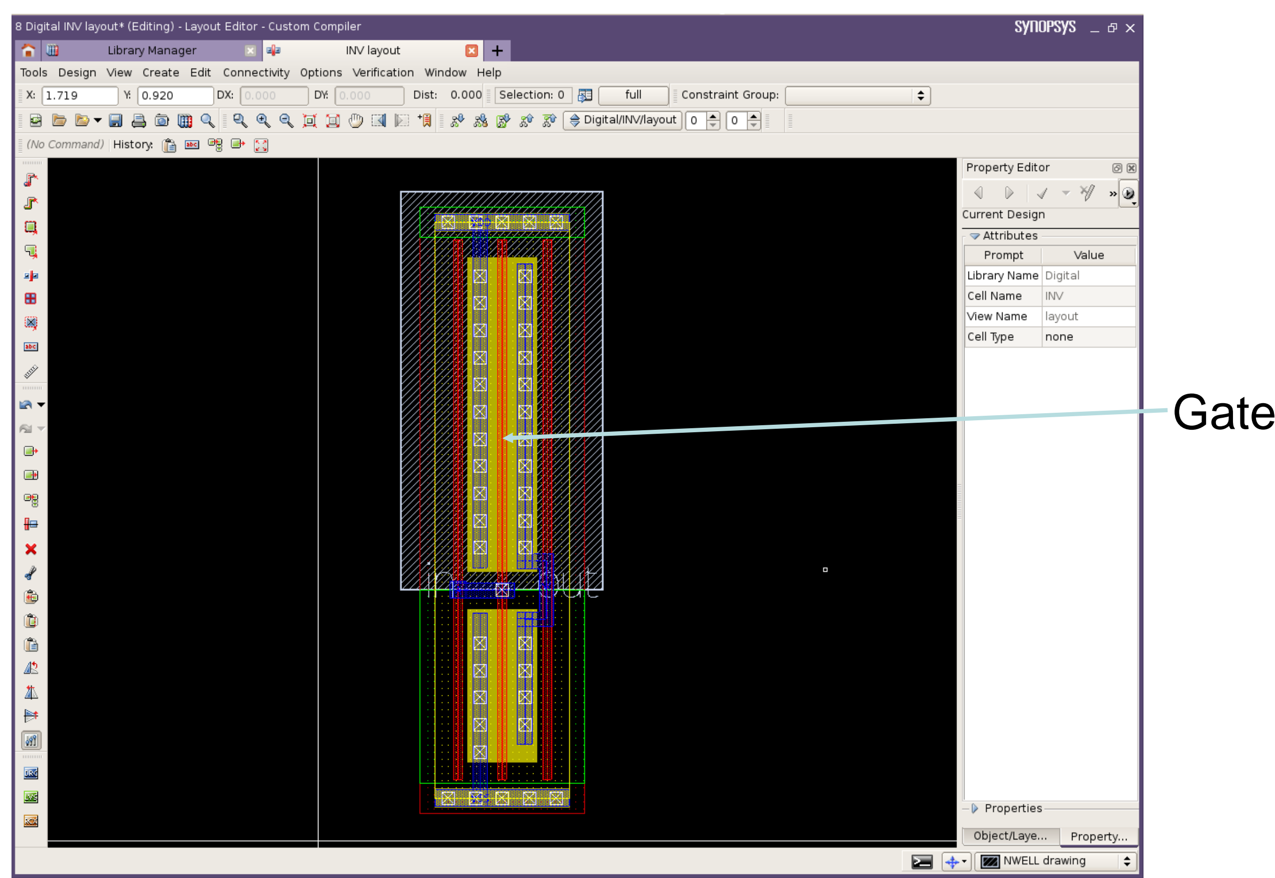
Layers: N-Well



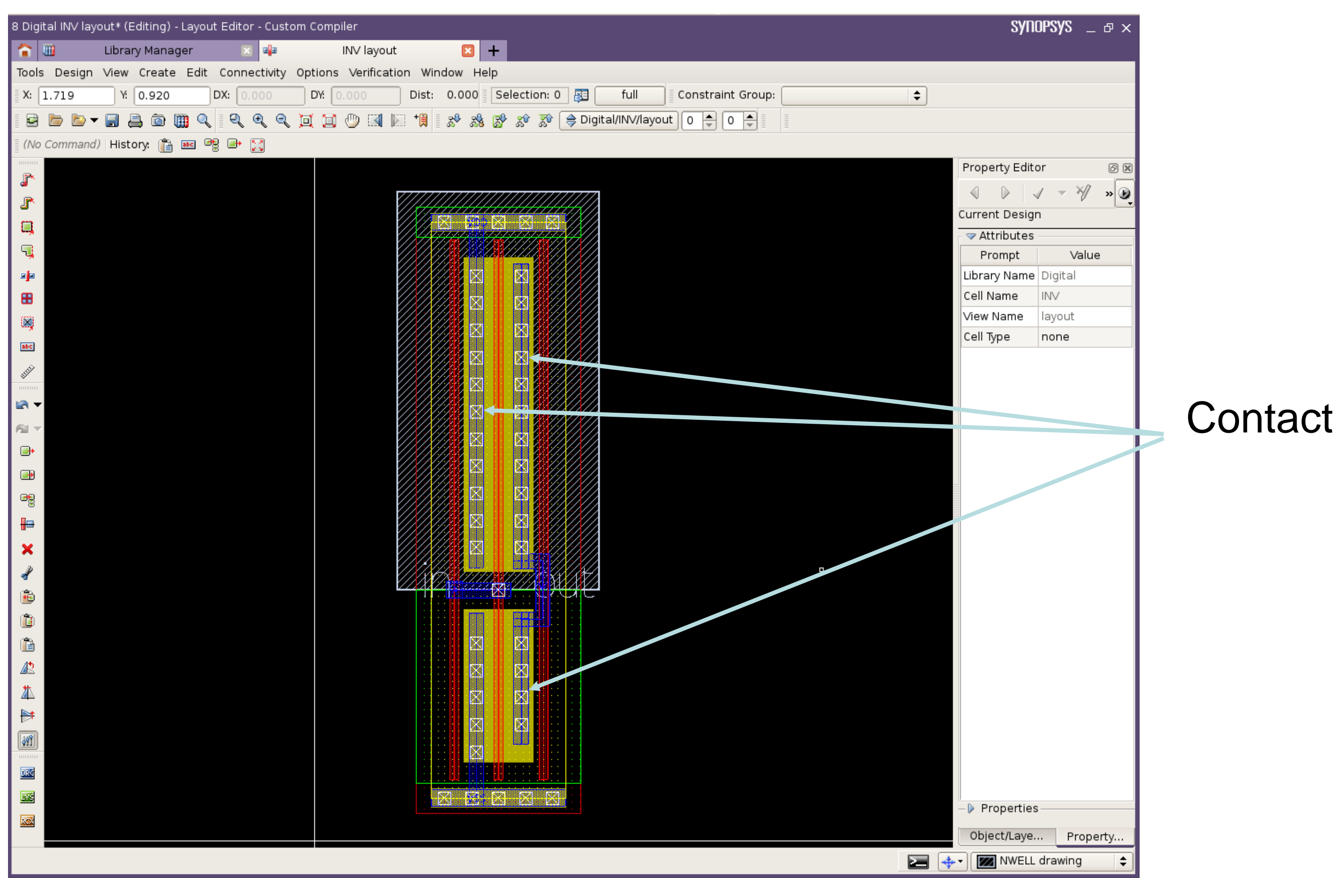
Layers: Active



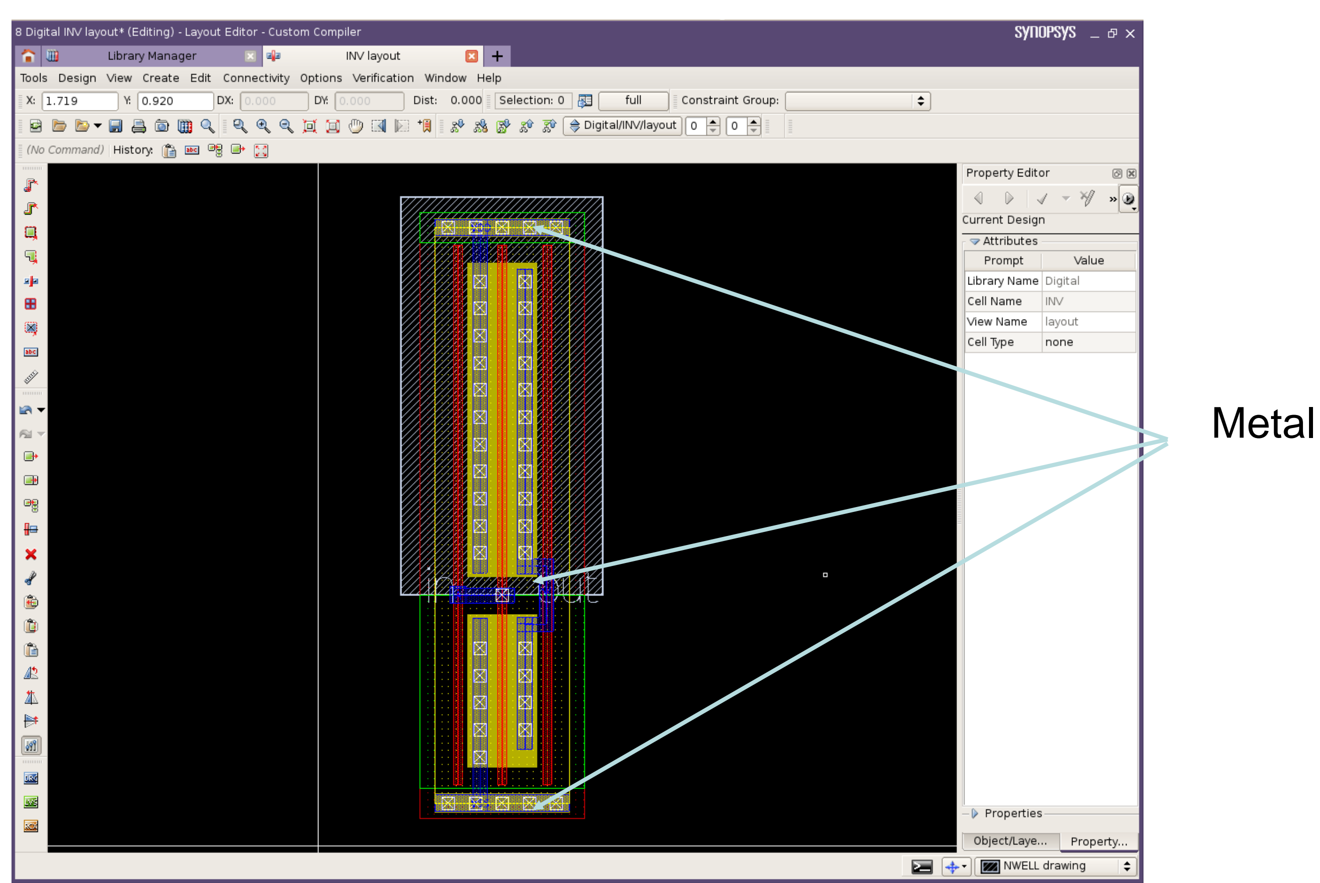
Layers: Gate



Layers: Contact



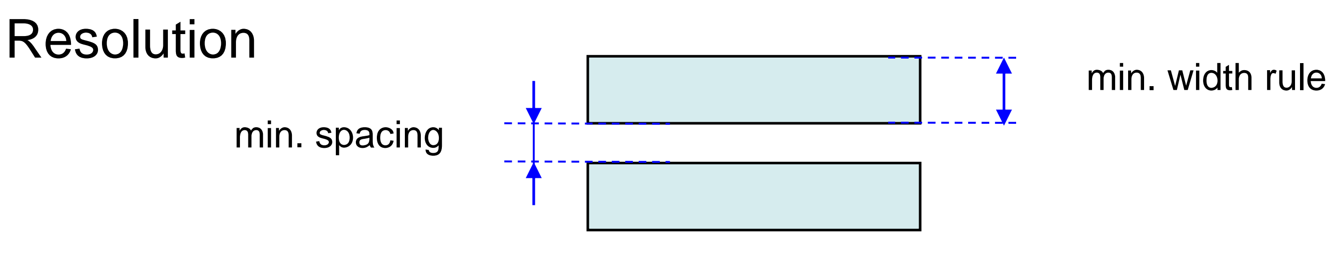
Layers: Metal



Design Rules: Necessity

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Rules constructed to ensure that design works even when small fabrication errors occur

Design Rules: Example



Alignment

min. poly width

min. poly overlap of diffusion

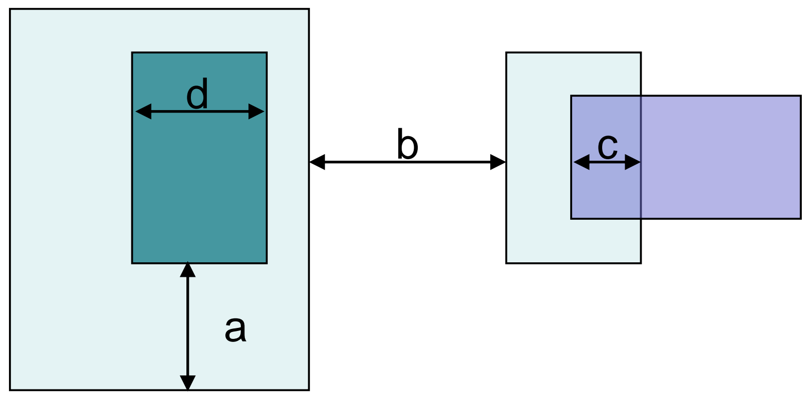
exact contact size

min. contact overlap

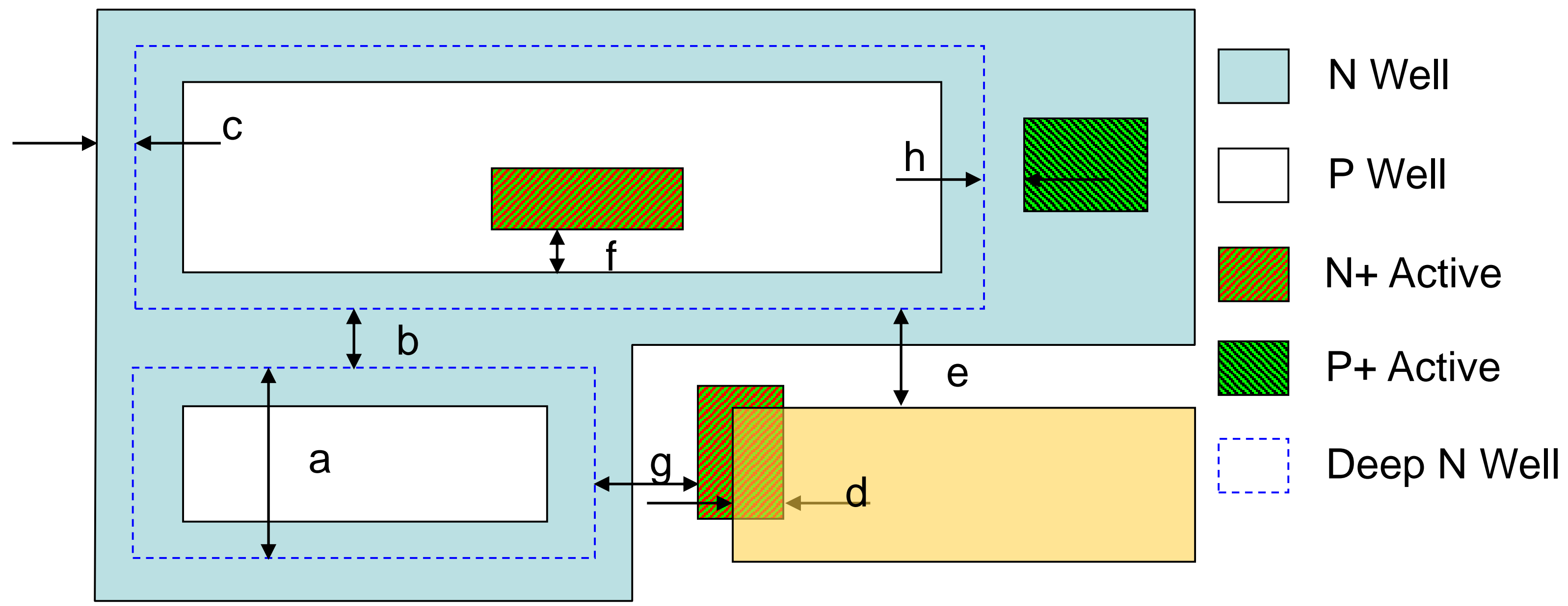
min. gate to contact spacing

Design Rules: Example (2)

a. Minimum enclosure in the result of combination of dopant or overhead layers
b. Minimum spaces between objects on the same layer to ensure they will not short after fabrication
c. Provision of minimum overlap of layers
d. Minimum dimensions of objects on each layer to maintain that object after fabrication



Design Rules: Example (3)



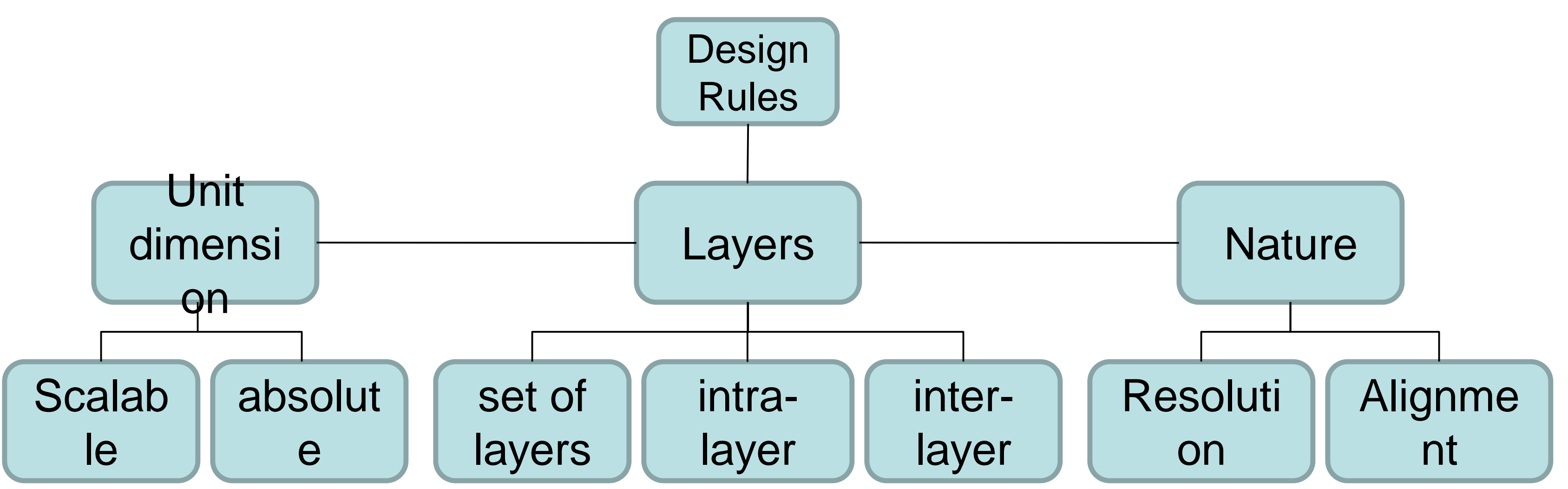
a – minimum width

b, e, g, h – minimum spacing

c, f – minimum enclosure

d – minimum overlap

Design Rules: Classification



Lambda (l) units:

- It is half the drawn gate length (poly width)
- All other design rules are expressed in whole multiples of l

- poly width 0.13mm
- poly spacing 0.2mm
- metal width 0.2mm
- metal spacing 0.2mm

- relations between objects in the same layer

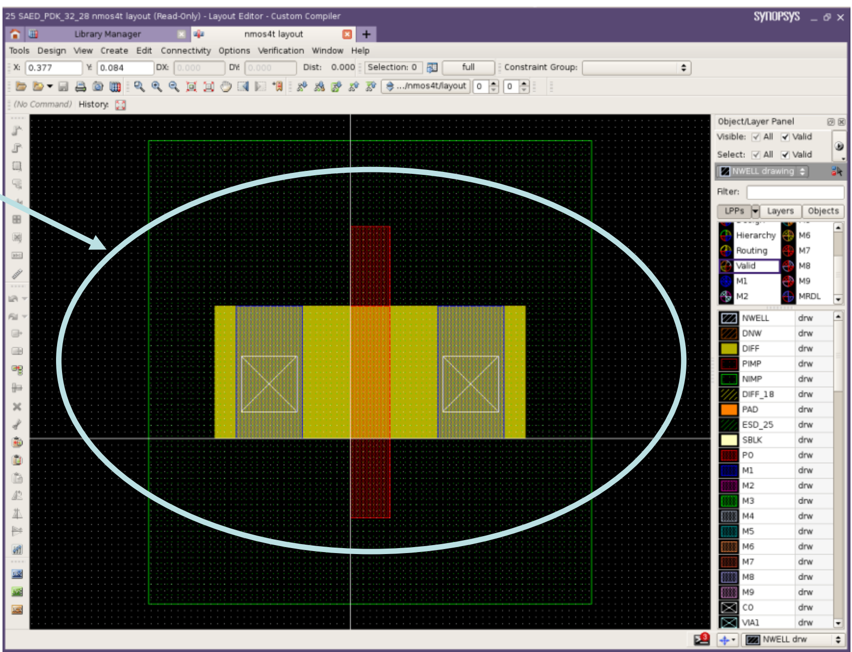
- relations between objects on different layers

- width and spacing of lines on one layer

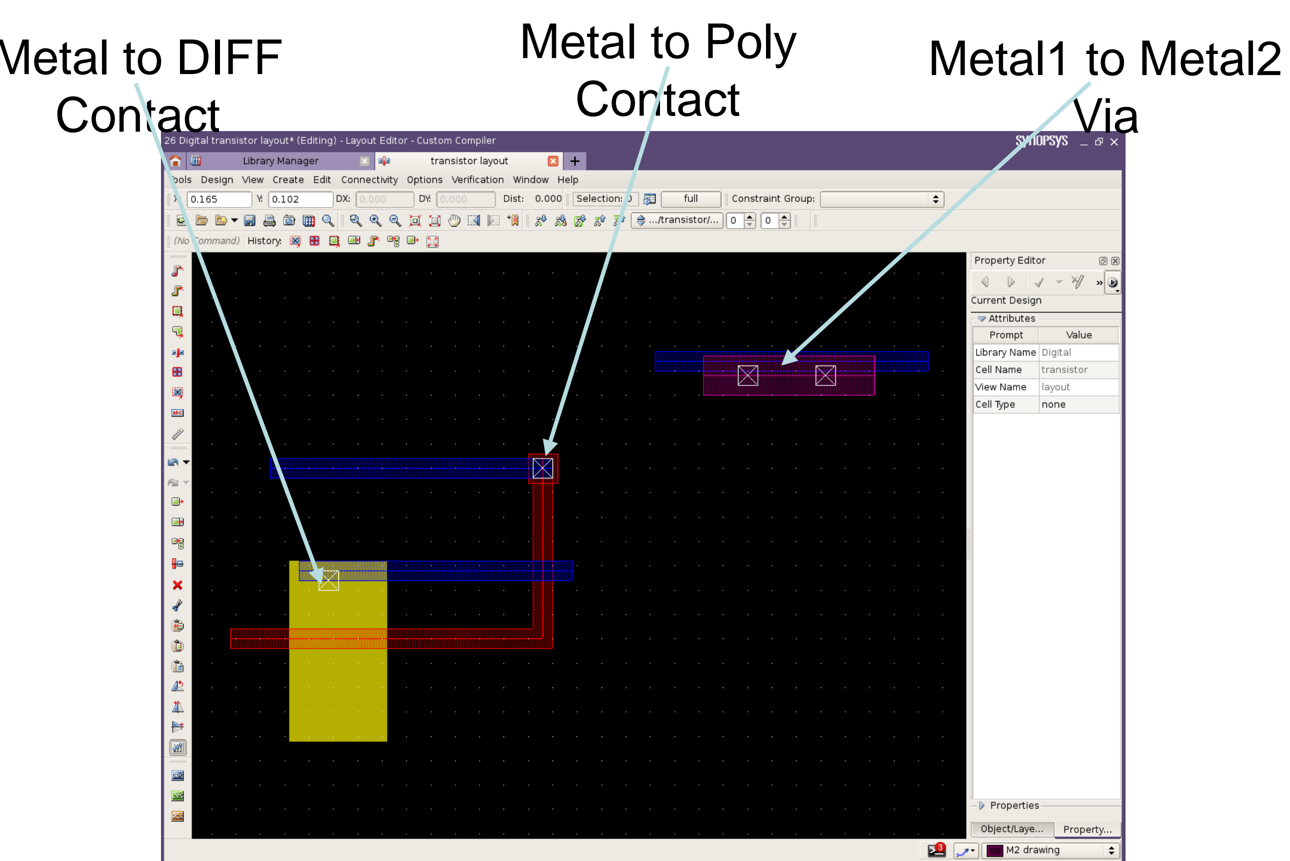
- to make sure interacting layers overlap (or don't)
- contact surround
- poly overlap of diff

Design Rules: Transistor Layout

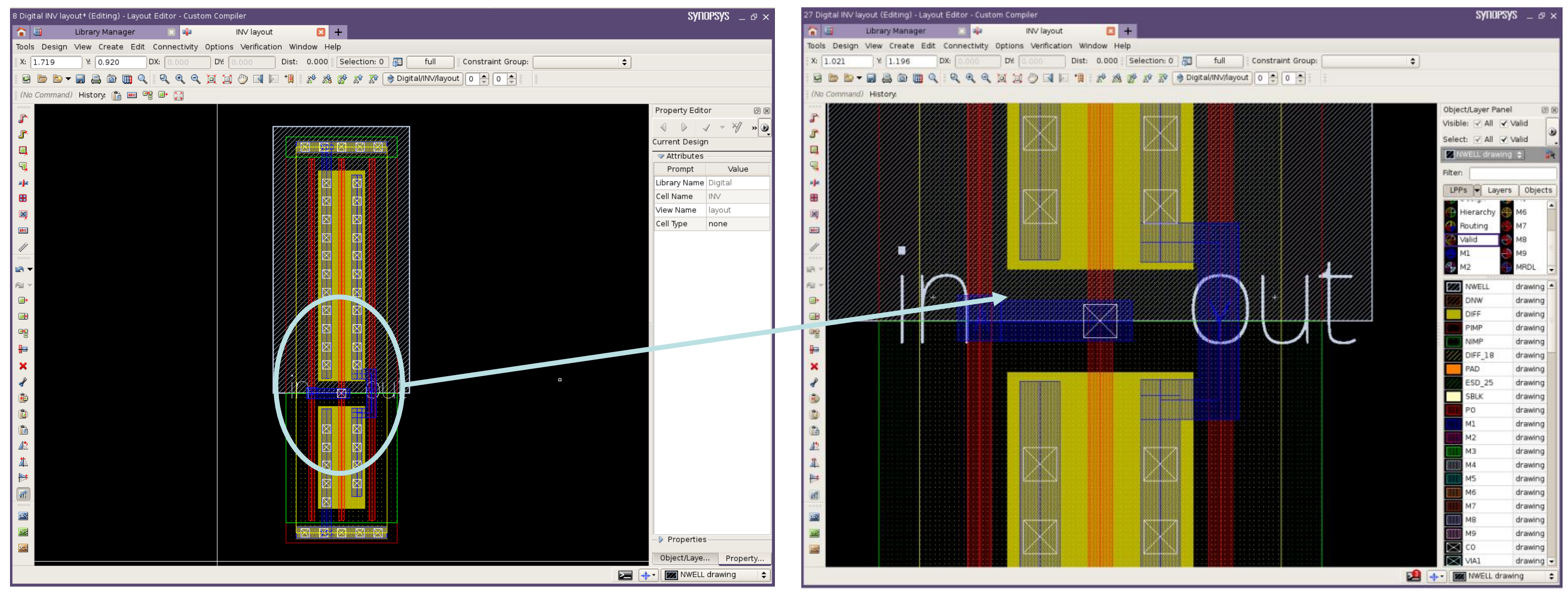
Transistor



Design Rules: Vias and Contacts

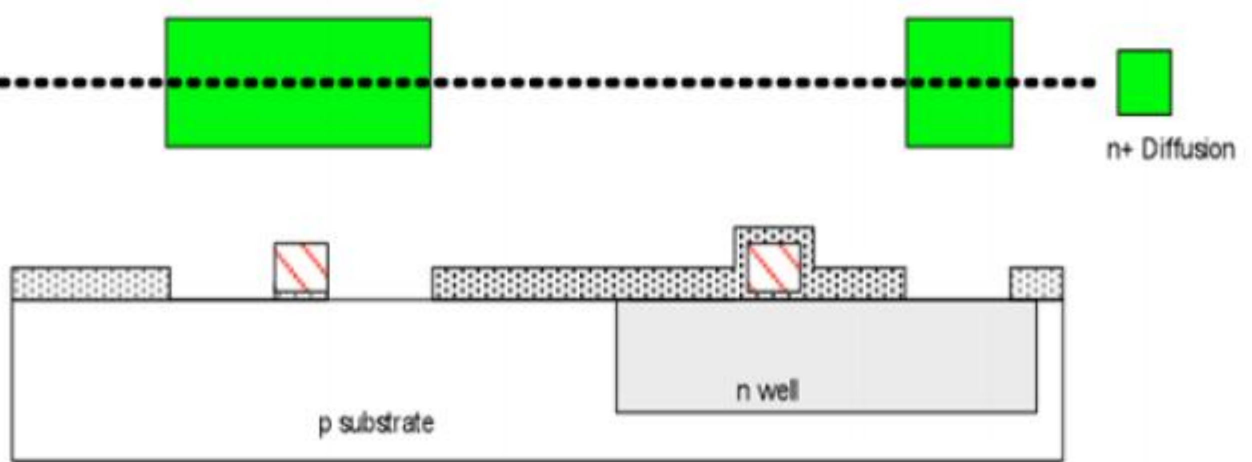


Design Rules: Design Rule Checker



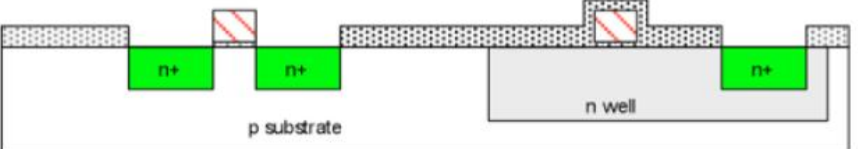
Formation of the n-diffusions

- Pattern oxide and form n+ regions
- *Self-aligned process* (poysilicon gate) “blocks” diffusion under the gate
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing

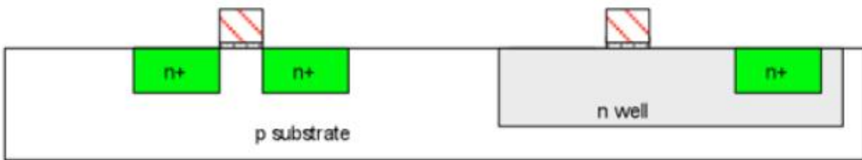


The n-diffusions

- Historically dopants were diffused
- Usually ion implantation today (but regions are still called diffusion)

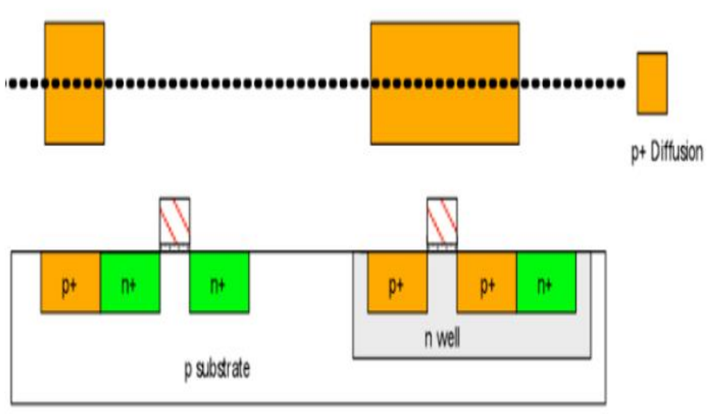


- Strip off oxide to complete patterning step



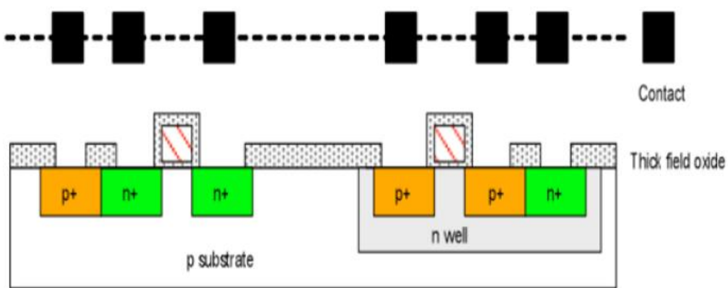
The p-diffusions

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



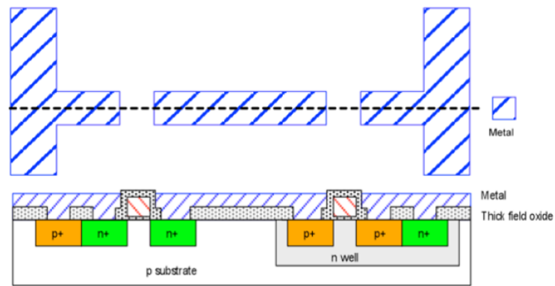
Contacts

- Now we need to create the devices' terminals
- Cover chip with thick field oxide (FOX)
- Etch oxide where contact cuts are needed

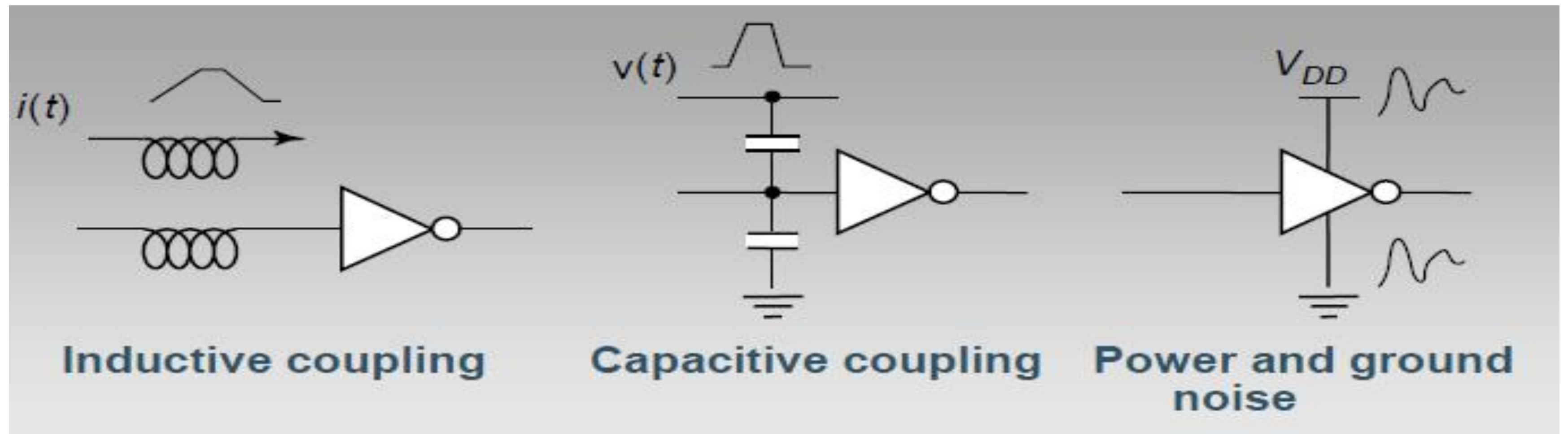


Metallization

- Sputter on aluminum over whole wafer, filling the contacts as well
- Pattern to remove excess metal, leaving wires



Design Metrics - Reliability—Noise in Digital Integrated Circuits



- Will talk more about noise and reliability in coming sections

Design Metrics- Power Dissipation

- Instantaneous power:
- $p(t) = v(t)i(t) = V_{supply}i(t)$
- Peak power:
- $P_{peak} = V_{supply}i_{peak}$
- Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

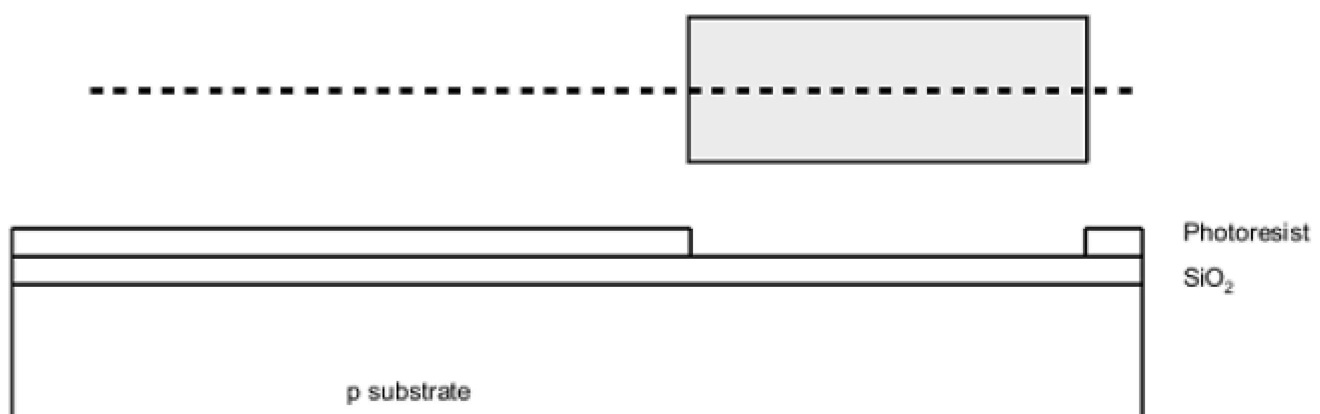
- Extra slides …. reading

Deposit silicon-oxide and photoresist

- Photoresist is a light-sensitive organic polymer
- Softens where exposed to light

Photo-Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



Etching

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone: nasty stuff!!!
- Only attacks oxide where resist has been exposed

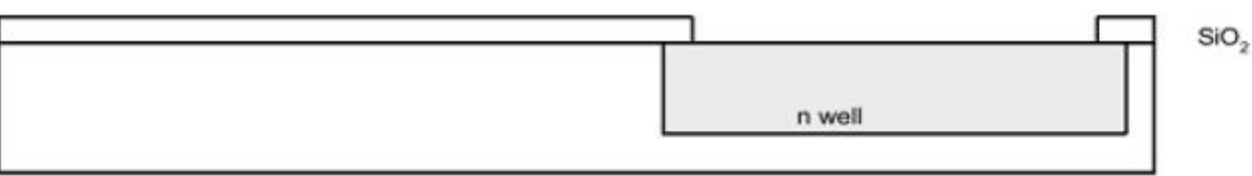
Photoresist

SiO_2

p substrate

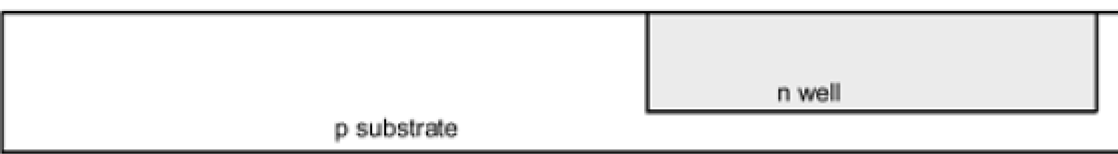
The n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



Strip protective oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

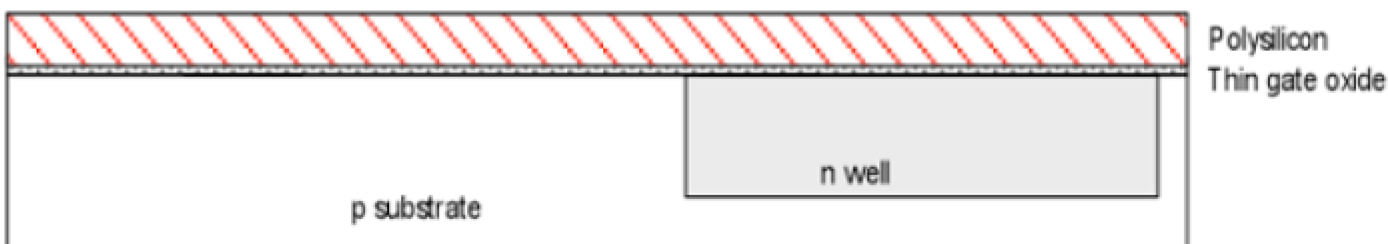


Gate oxide and Polysilicon

- Deposit very thin layer of gate oxide

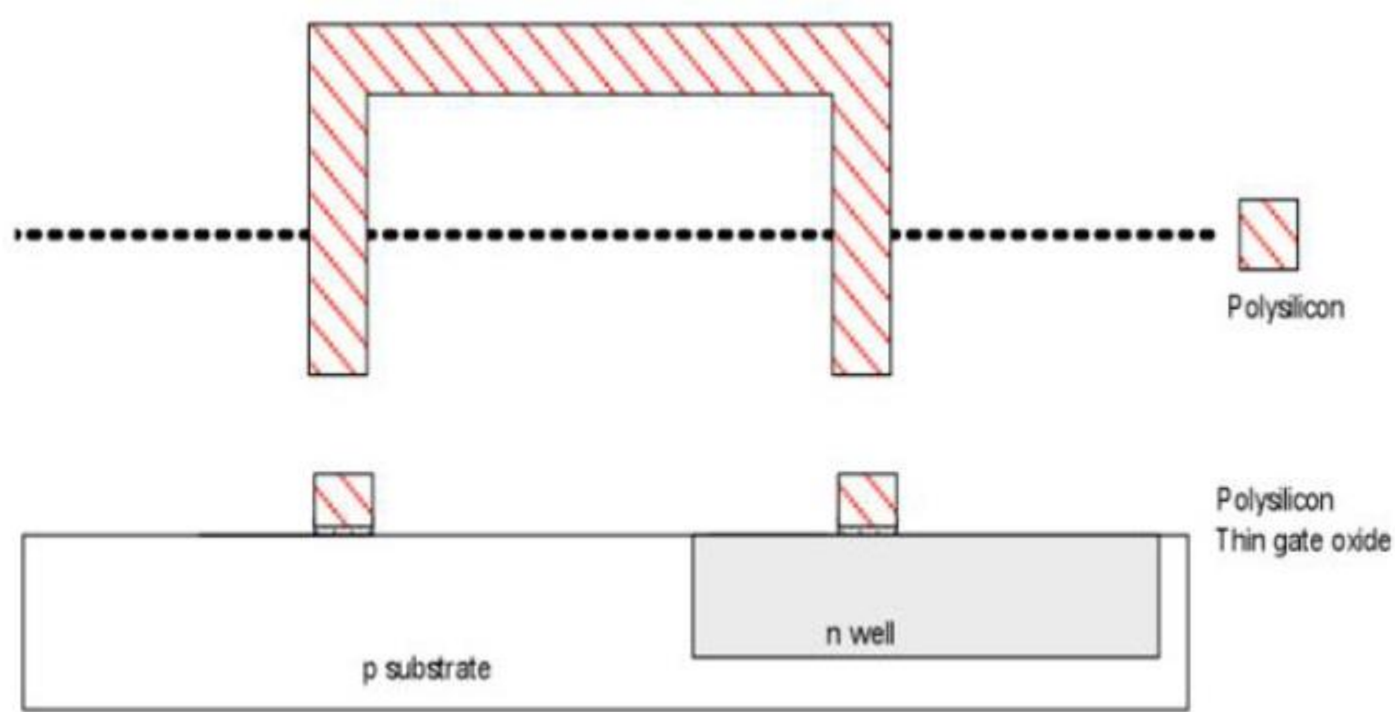
  < 20 Å (6-7 atomic layers)

- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



Polysilicon patterning

- Use same lithography process to pattern polysilicon



Self-aligned polysilicon gate process

- The polysilicon gate serves as a mask to allow precise alignment of the source and drain with the gate
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- n-diffusion forms nMOS source, drain, and n-well contact